Stan Mazor: Reflections on Gordon Moore, Fairchild, and Intel

Interviewed by Brian Berg

2 May 2023
Stan Mazor’s Career

1960  San Francisco State University
1964  Fairchild (Semiconductor)
1969  Intel (Semiconductor)
1983  Silicon Compilers (CAD)
1988  Synopsys (CAD)
1996  BEA Systems (Middleware)
1998  Cadabra/Numerical (CAD)
2003  Retired (Author)
Stan Mazor: 1958 (Age 17)

Oakland Tribune
OAKLAND, CALIFORNIA, WEDNESDAY, OCTOBER 22, 1958

LEADERS—Members of the new high school Oakland City Council are (front from left) Carolina Skarsten, Larry Slocumb, Technical High; Stan Mazor, Oakland High; Bill Beldrop O’Dowd High; Henry Mase, Bishop O’Dowd High; Lulu Mae Crow, Monte High; (rear from left) Lena Hunter, Linda Bright and Marian Hansen, St. Mary High; Frederick Donley III and Lee Pratt, Castlemont High, and Stan.
Statesmen Getting Out Vote

By BRENDA COLLINS

"JUNIOR Statesmen have worked too much within the organization and not enough outside it," declares Stan Mazor of Oakland, state governor. "We wish to be a service organization, in addition to an educational one."

Chapters from around the state are already implementing the new policy set down by their governor. Today they helped get out the vote. In many areas of the state members baby sat while mothers voted, and they drove others to their polling places. Statesmen also distributed leaflets to citizens urging them to cast their ballots.

A second project, completed Friday, was a political preference poll, in which students from 50 California high schools participated. Candidates and issues were discussed in history and American problems classes before the voting.

Jr. Statesman Annual Ball
Stan Mazor: 1959 (Age 18)

The Junior Statesman

Mazor Becomes Lobbyist
Governor to receive credential soon

Applications for Prof. Rogers Award sent out

Gov. Brown

Pres. Harry Truman

Jr. Prom Fremont Hi
San Francisco State Univ.: 1960-1963

- Machine Shop: helicopter project
- Philosophy – Formal logic – deMorgan’s theorem
- Advanced Calculus – epsylon/delta theory
- Probability/Statistics – Normal distribution
- Assembly language programming – interpreter
Stan Mazor at SFSU: 1963 (Age 21)

Learned programming
Studied Computer Design
Learned some:
  - statistics
  - bookkeeping
  - economics
  - philosophy
  - selling (job)
  - No major
  - No required classes
  - No degree
Stan Mazor at SFSU: 1963 (Age 21): Working on an IBM 1620
Stan Mazor in Silicon Valley: 1964 (Age 23)
Dual Inline Packages (DIP)
Chip in Package
Silicon Wafer
Integrated Circuit (IC) Chip

• Collection of connected transistors
  o Hoerni’s “planar” process 1960
  o Noyce (Fairchild) CTuL (micro logic)
  o Kilby (TI) TTL Nobel Prize (2000)

• Limits (1970):
  o Design and layout complexity (no CAD)
  o On chip wiring (1 metal layer)
  o Package pins 14 (then 16)
  o Power dissipation (< 1 Watt)
Sorted Wafer

300 + processing steps
20+ photographic steps
~3 months to make

Ink marks defective dice

Defects:
- wafer material defects
- processing defects
- statistical limits
Yield Estimate: 4X Larger Die

Bigger Chip = Lots of stuff  Few good ones

Yield \( \frac{25}{81} = 30\% \)

(of 81+ possible)
Yield Estimate: 25X Larger Die

Almost 1 good (of 16 possible)

Zero Yield

Big Chips = Lots of stuff

No good chips
Transistor Cost v. Density: Bathtub Curve
Chip Object Sizes

- 100 Mhz Pentium
- 2 Ghz Penryn
- first microcomputer (1/10th human hair diameter)

2000 nanometer = 2.0 micron

- 1000 nm
- 800 nm

- 350 nm
- 250 nm
- 180 nm
- 130 nm
- 70 nm
- 50 nm

Wavelength of light

Timeline:
- 1985
- 1990
- 1995
- 2000
- 2005
- 2008
Gordon Moore’s 1965 Observation at Fairchild (aka, “Moore’s Law”)

- Select chip Cost
- Density increase
  \(~32x\) in 5 years
  Doubles yearly
4k Bits Static RAM (chips)
Another View of Moore’s Law
Reflections on Gordon Moore by Bill Davidow of Mohr Davidow Ventures
Gordon Moore’s Fairchild R&D Projects (1966)

- Micro Mosaic: standard cells
- Micro Matrix: gate arrays
- Fairsim: logic simulator and CAD tools
- **Symbol**: large scale computer
- Op Amp: analog circuit
Fairchild Symbol 2R Computer Intro (1968)

Use 10x more logic
Plan for future LSI
20 guys for 5 years

Features of the Symbol computer:

- New Symbol programming language
- Hardware directly executed Symbol source code
- Compiler and operating system built with hardware
- Memory controller provided virtual memory
- US Patent 3,647,348 (Stan was co-inventor)
- Hardware supported dynamically-varying sized data
Printed Circuit Board (PCB)

Printed wires

200 IC’s
Symbol Program Example

Y = “is good”;  
Y = “ is much better than it was”;  
Y = 3/2;  
Y[2] = <18, 24,36>;
Memory Operations

- **Assign group**—AG. This operation allocated a new group from the storage free list, (allocated a new page if needed), and returned the address of the first word in the group.

- **Store and assign**—SA. This operation stored the data word at the address sent, and returned the next sequential address for the following word in the same group. If the group was full, it allocated another group from the free space pool, and linked the groups together, and returned the address of the next free location in the group.

- **Fetch and follow**—FF. This operation fetched the data word at the address given and returned the next sequential address of data, if in another group, it followed the link. If this was the end, it returned a null address.
Integrated Circuit (IC)

• Limits (1970):
  o Design and layout complexity (weak CAD)
  o On chip wiring (1 metal layer)
  o Package pins 14 (then 16)
  o Power dissipation (< 1 Watt)
  o Logic gates and 4-bit latch
1969: Move from Fairchild to Intel
MCS-4 (My Memories)

• ROM memory  4001
• RAM memory  4002
• Shift register (memory chip)  4003
Glass Teletype (1970)

- Competitive cost vs teletype
- Beehive, Wyle, Hazeltine, Datapoint
- Memory data: 25 lines x 80 char/line
  Serial 2,000 chars x 6 bits = 12k bits
- Shift register memory chips
- Datapoint 2200 8-bit computer
- Intel 8008 CPU chip (patents)
Ideal Memory Chip

- 1k bits ‘same’ cell layout
- Short wires connect neighbors
- 2 data pins IN and OUT
Ideal Memory Chip Layout (S)

The Shift Register

IN

OUT
Ideal Memory Chip and PCB

- All chips are 1k SR’s
- Short wires connect neighbors
- 2 data pins IN and OUT
Random Access Read Only Memory (ROM)

- Layout Mask sets (writes) data
- Random access (Address In) selects data
- **Chip Select** enables Data **out**
Photo Lithography

![Diagram showing the process of Photo Lithography with a light source, lens, mask, pattern image, and wafer with 'photo resist'].
Busicom Calculator MCS-4 Chips

CPU Acc, 16 index regs, 4-bit, 45 instr.  
4 ROM  256 x 8 = 1k program code  
2 RAM  4 register x 16 digit x  = 8 numbers  
Serial 14 digit floating point arithmetic  
Need I/O signals for keyboard and printer  
6 memory chips x 4 pins = 24 I/O pins  
15 V PMOS SiGate  

Pins are valuable, logic is cheap
12-bit Program Counter \( \text{PC} (\text{CCCC} \text{HHHH} \text{LLLL}) \)
8-bit Memory Address Register \( \text{MAR} \) gets \((\text{LLLL}, \text{HHHH})\) :c1, c2
ROM 256 x 8; 8 bits read (every ROM) using MAR :c3
ROM has 4-bit ID code CCCC :c3
CPU sends chip ID CCCC to all ROM’s :c3
The selected ROM sends 8-bits (op code) to CPU :c4, c5
No Chip Select (CS pin) on ROM (CCCC selects one ROM ID)
4001 ROM: 4-bit I/O port

Each 4001 ROM has 4 bit I/O port (pins)
CPU executes Read/Write of ROM port
ROM sees/decodes op code : c4, c5 (no control pins)
CPU op: RDR reads ROM port 4-bits into ACC
CPU op: SRC selects a ROM chip port (previously)
IBM Core Memory Unit

- Extends Main Frame memory
- Read/Write memory ops (transparent)
Random Access Memory (DRAM)

- Random access (Address In) selects data
- Data in and Data out
- Read out or Write data in
4002 RAM: 4 Registers

- RAM ID is 0-3 built-in
4002 RAM

Read/Write RAM data (Data in, Data out)
No Read or Write pin on 4002 RAM
Write ACC to 4-bit port
No Write port pin on 4002 RAM
4004 CPU Read Port Instructions

<table>
<thead>
<tr>
<th>E9</th>
<th>ROM</th>
<th>1110 1001</th>
<th>Read the previously selected RAM main memory character into the accumulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>EA</td>
<td>RDR</td>
<td>1110 1010</td>
<td>Read the contents of the previously selected ROM input port into the accumulator (I/O Lines)</td>
</tr>
</tbody>
</table>
8008 Microprocessor Spec

Written @ Intel 1971

Design issues:
- die size
- power dissipation
- package pin count
- testability

Patented by TI

CTC CPU PRELIMINARY DESCRIPTION

The CPU is an 8 bit parallel central processor unit for a computer system. It can be interfaced with various memories having capacities up to 16k bytes.

The processor communicates over an 8 bit data and address bus and uses 2 input and 2 output leads for control. Time multiplying of the data bus allows control information, in 8 bit addresses and data to be transmitted between the CPU and memory.

The CPU contains two 8-bit data registers and a 14-bit program counter. An 8-bit parallel binary adder-subtractor implements arithmetic & logical operations. A memory stack containing seven 14-bit words is internally used to store program subroutine addresses.

The CPU contains look to implement a variety of register transfer, arithmetic, control and logical instructions. Some instructions are coded in one byte (8 bits), data immediate instruction use 2 bytes; jump instructions utilize 3 bytes. Operating between 1 & 2 microsecond cycle time the CPU executes non memory referencing instructions in under 10 microseconds.
Hal Feeney, designer

- **8008 Microprocessor: 1972**
- **Registers:** 7 x 8-bits
- **PC Stack:** 8 x 14-bits
- **Instruction Decoder**
- **8-bit ALU**
- **18 pin package**
- **14 volts**
- **1/2 Watt**
Intel 8080 Chip: 1974

40-pin DIP
5 Volts
3/4 Watt

M. Shima (island)
Intel Microprocessor Credits

4004 Microprocessor (1971)
• **Hoff**: MCS-4 architecture and instruction set (before Stan joined)
• **Mazor**: added 4 instr. (FIN, JIN, +2); wrote interpreter and code
• **Faggin**: did all logic, circuit design, layout, testing, and chip plans
• **Shima**: Busicom calculator designer: all coding, assisted layout verification

8008 Microprocessor (1972)
• **Mazor**: proposed 8-bit CPU
• **Faggin**: supervised (Feeney) (1973 TI patent: US 3,757,306)

8080 Microprocessor (1974)
• **Faggin, Shima, Mazor** (1977 Intel patent: US 4,010,449)
Conclusions

• Known physical limits may be overcome (maybe not)
  Moore's law will slow down
  Chip heat and energy issues prevail
• Technology requires large financial investment
  Invest only if there is a market
  New technologies enable new markets
• Existing approaches tend to saturate
• Some new directions identified, but are unproven
<table>
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<tr>
<th>Company</th>
<th>Patent Information</th>
</tr>
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<tbody>
<tr>
<td><strong>TI</strong></td>
<td>awarded US Patent 3,757,306 on September 4, 1973 for the single-chip 8-bit CPU (8008) 8 Claims: CPU</td>
</tr>
<tr>
<td><strong>Intel</strong></td>
<td>awarded US Patent 4,010,449 on March 1, 1977 for &quot;MOS Computer&quot; (8080) Federico Faggin, M. Shima, Stan Mazor 2 Claims: coding</td>
</tr>
</tbody>
</table>
1983: Silicon Compilers

- Founded in 1981 by Carver Mead, David L. Johannsen, and Edmund K. Cheng
Mazor’s writings:

- Intel 4004: 2005
- Intel 8008: 2006
- Intel 8080: 2007
- Symbol Computer: 2008
- Magnavox video game: 2009
- Intel 8086: 2010
Recognitions

- 1996: National Inventors Hall of Fame
- 1997: Kyoto Prize
- 2000: Robert N. Noyce Award
- 2009: Computer History Museum Fellow
- 2009: National Medal of Technology and Innovation
  - From Pres. Obama, with Ted Hoff and Federico Faggin
  - “for the conception, design, development, and application of the first microcomputer, a universal building block that enabled a multitude of novel digital electronic systems”