Stan Mazor: Reflections on Gordon Moore, Fairchild, and Intel

Interviewed by Brian Berg

2 May 2023

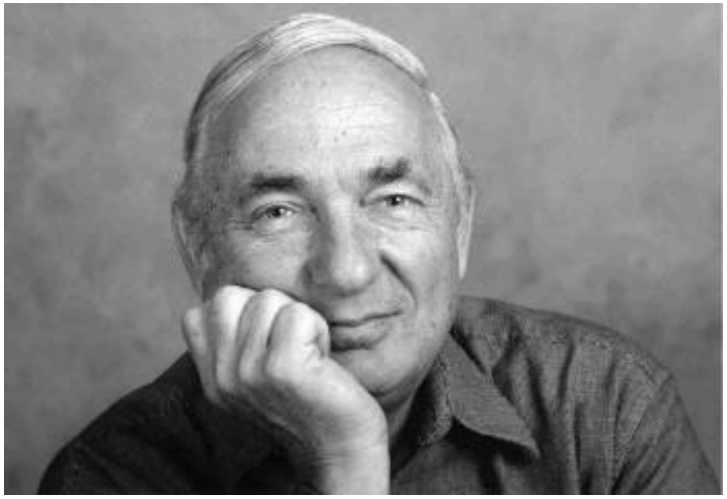
IEEE-CNSV

Consultants' Network of Silicon Valley

IEEE

Advancing Technology for Humanity

Stan Mazor's Career



1960 San Francisco State University
1964 Fairchild (Semiconductor)
1969 Intel (Semiconductor)
1983 Silicon Compilers (CAD)
1988 Synopsys (CAD)
1996 BEA Systems (Middleware)
1998 Cadabra/Numerical (CAD)
2003 Retired (Author)

Stan Mazor: 1958 (Age 17)

Oakland Tribune

ESTABLISHED FEBRUARY 21, 1874

ASSOCIATED PRESS ... WIREPHOTO ... UNITED PRESS INTERNATIONAL ... CHICAGO DAILY NEWS FOREIGN SERVICE

OAKLAND, CALIFORNIA, WEDNESDAY, OCTOBER 22, 1958

Stan

EADERS—Members of the new high school Oakland City Council are (front, from left) Carolin Skarsten, High; Larry Slocomb, Technical High; Stan Mazor, Oakland High; Bill Bajd- op O'Dowd High; Henry Mase, Bishop O'Dowd High; Lilu Mae Crow, Mc- High; (rear from left) Lena Hunter, Linda Bright and Marian Hansen, St.

Stan Mazor: 1958 (Age 17)

Bobby Lobby

Statesmen Getting Out Vote

By BRENDA COLLINS

"JUNIOR Statesmen have worked too much within the organization and not enough outside it," declares Stan Mazor of Oakland, state governor.

"We wish to be a service organization, in addition to an educational one."

Chapters from around the state are already implementing the new policy set down by their governor.

Today they helped get out the vote. In many areas of the state members baby sat while mothers voted, and they drove others to their polling places. Statesmen also distributed leaflets to citizens urging them to cast their ballots.

A second project, completed Friday, was a political preference poll, in which students from 50 California high schools participated. Candidates and issues were discussed in history and American problems classes before the voting.

has also been a delegate to Boys' State.

Moreover, he has done his share of work in the political campaign—for both parties! Despite his interest in politics,

Mr. and Mr
Bullard Ave
Debbie, who
Oakland Hig
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McChesney
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squires Mau

Two other
Oakland Hi
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Jr. Statesman Annual Ball

Stan Mazor: 1959 (Age 18)

The Junior Statesman

Second class mail privilege authorized at San Francisco, California — Annual subscription price .25

VOLUME XVI — FEBRUARY, 1959 — NUMBE

MAZOR BECOMES LOBBYIST

GOVERNOR TO RECEIVE CREDENTIAL SOON

The Governor of the Junior State, Stan Mazor, has become the first teenager to receive credentials for lobbying in Sacramento. Governor Mazor is thought to be the first teenaged lobbyist in the history of the United States.

As a "legislative advocate" Governor Mazor will express the opinions to committees of the California legislature on bills that pertain to [illegible] in this state. It is hoped that in the future Governor Mazor

APPLICATIONS FOR PROF ROGERS AWARD SENT OU

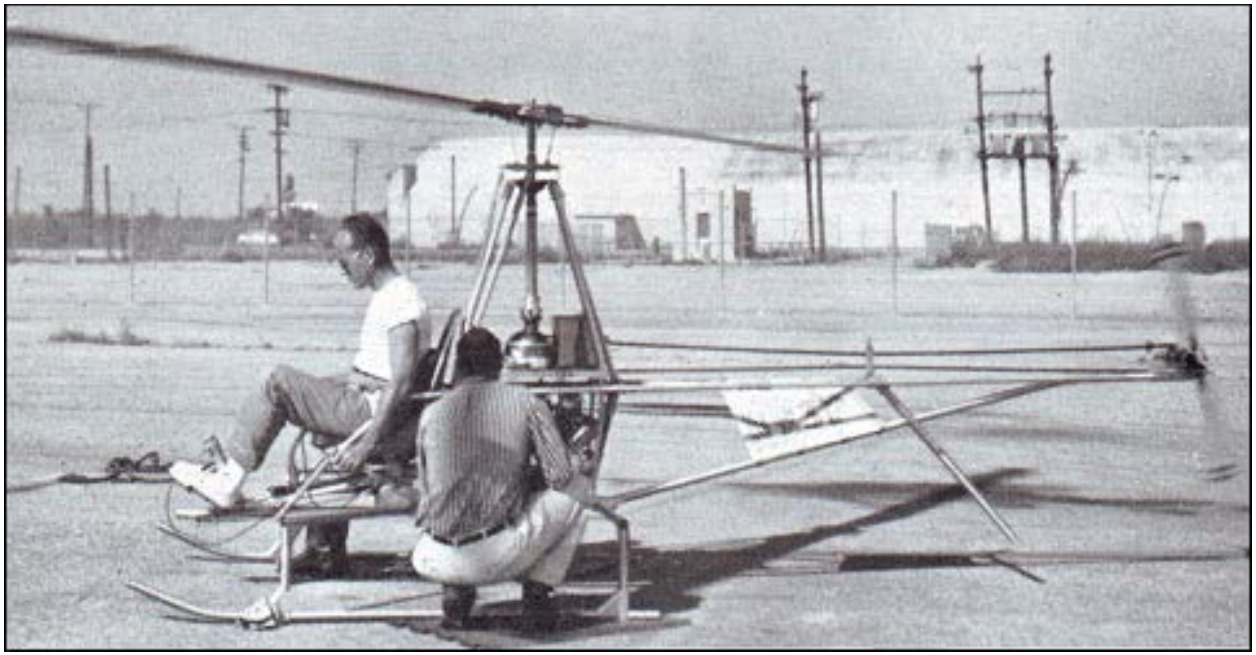
Formal applications fo 1958-59 E. A. Rogers Award be sent to all chapters within next month, according to Mancial, President of the C uate Statesmen.

All chapters are eligi compete for the award. The pre-requisite for considerat that a chapter must have on all constitutional amendr submitted to it. Mr. Mar speaking for the comm stated, "We urge all chapt apply, since they will bene the knowledge of their effe ness in relation to other ters."

The award is based on a tem of 100 points. Thirty sible points will be given fo ialative programs on chapte gion, and state levels, an conduct in sessions. Anot points will be possible for c ization, expansion, coope with regions, the state, and chapters. Thirty points w possible for activities, su service to the school an community, public rela and publicity, and a general balanced program. An o 10 possible points will be a for general improvement o petence, outstanding [illegible]

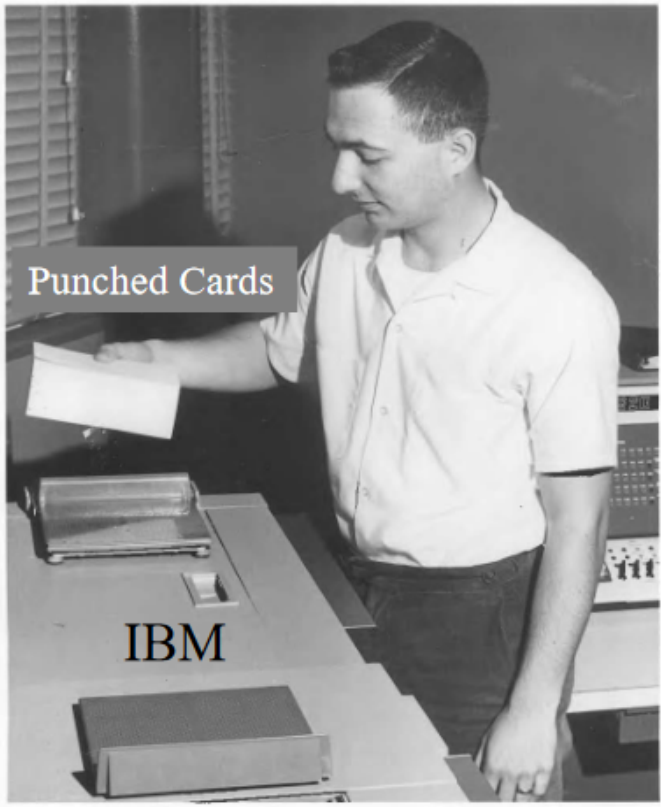
Jr. Prom Fremont Hi

San Francisco State Univ.: 1960-1963



- Machine Shop: **helicopter project**
- Philosophy –Formal logic—deMorgan's theorem
- Advanced Calculus---epsilon/delta theory
- Probability/Statistics—Normal distribution
- **Assembly language programming—**interpreter

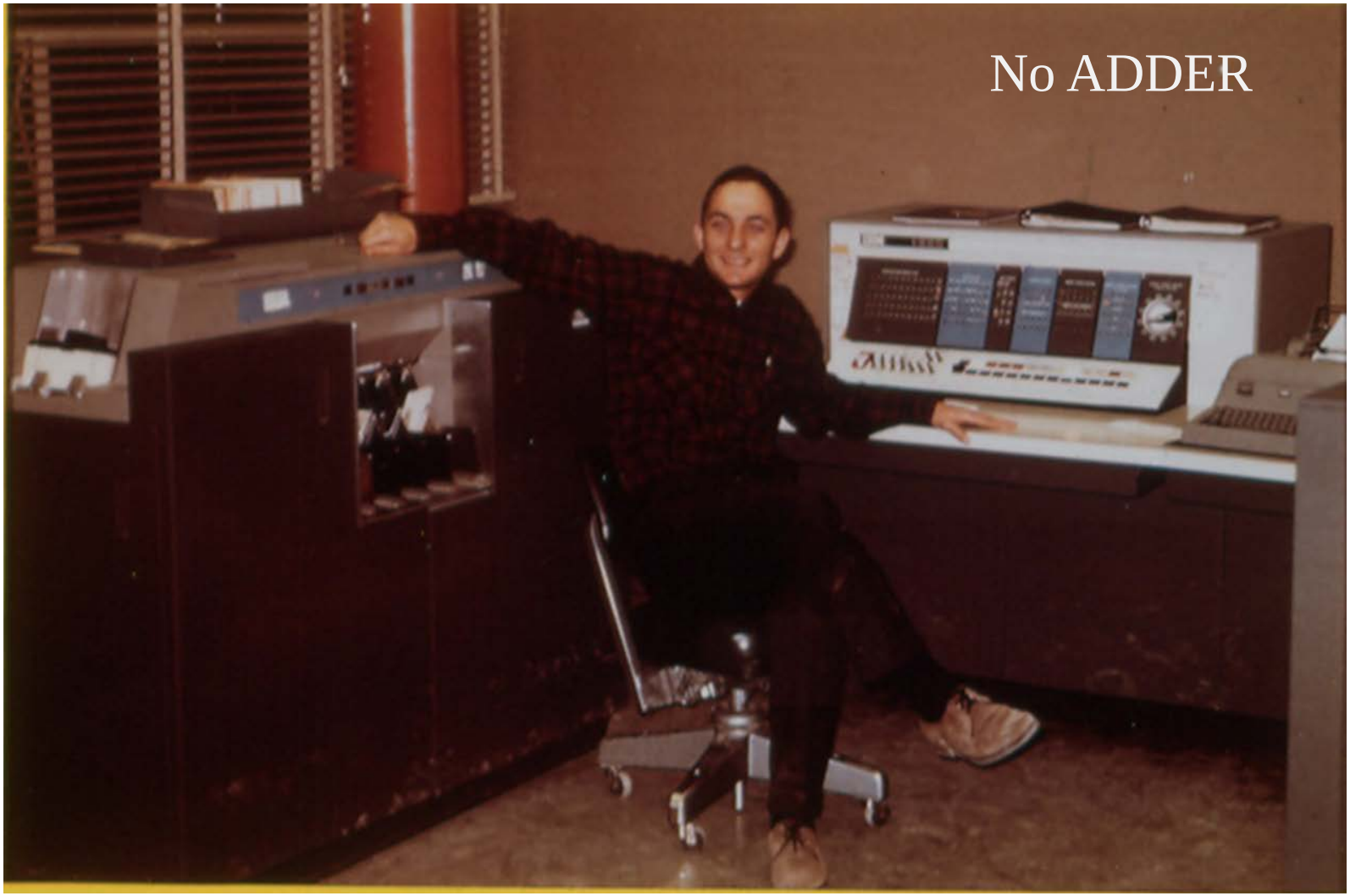
Stan Mazor at SFSU: 1963 (Age 21)



Learned programming
Studied Computer Design
Learned some:

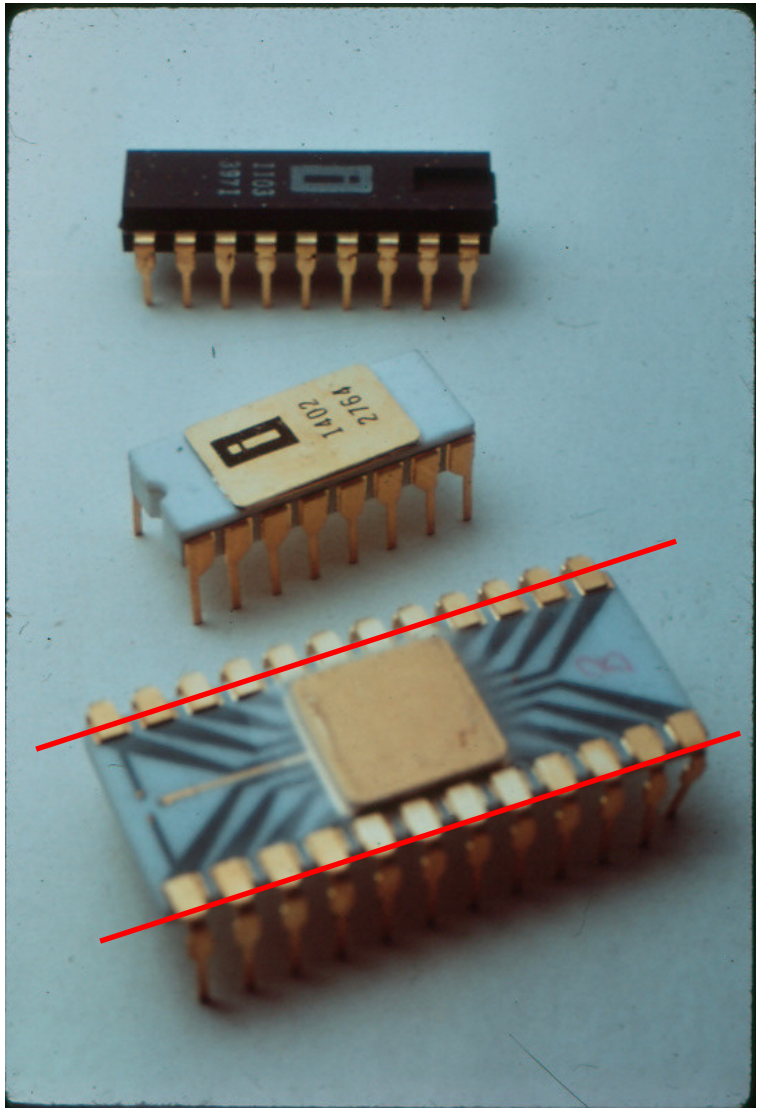
- statistics
- bookkeeping
- economics
- philosophy
- selling (job)
- *No major*
- *No required classes*
- *No degree*

Stan Mazor at SFSU: 1963 (Age 21): Working on an IBM 1620

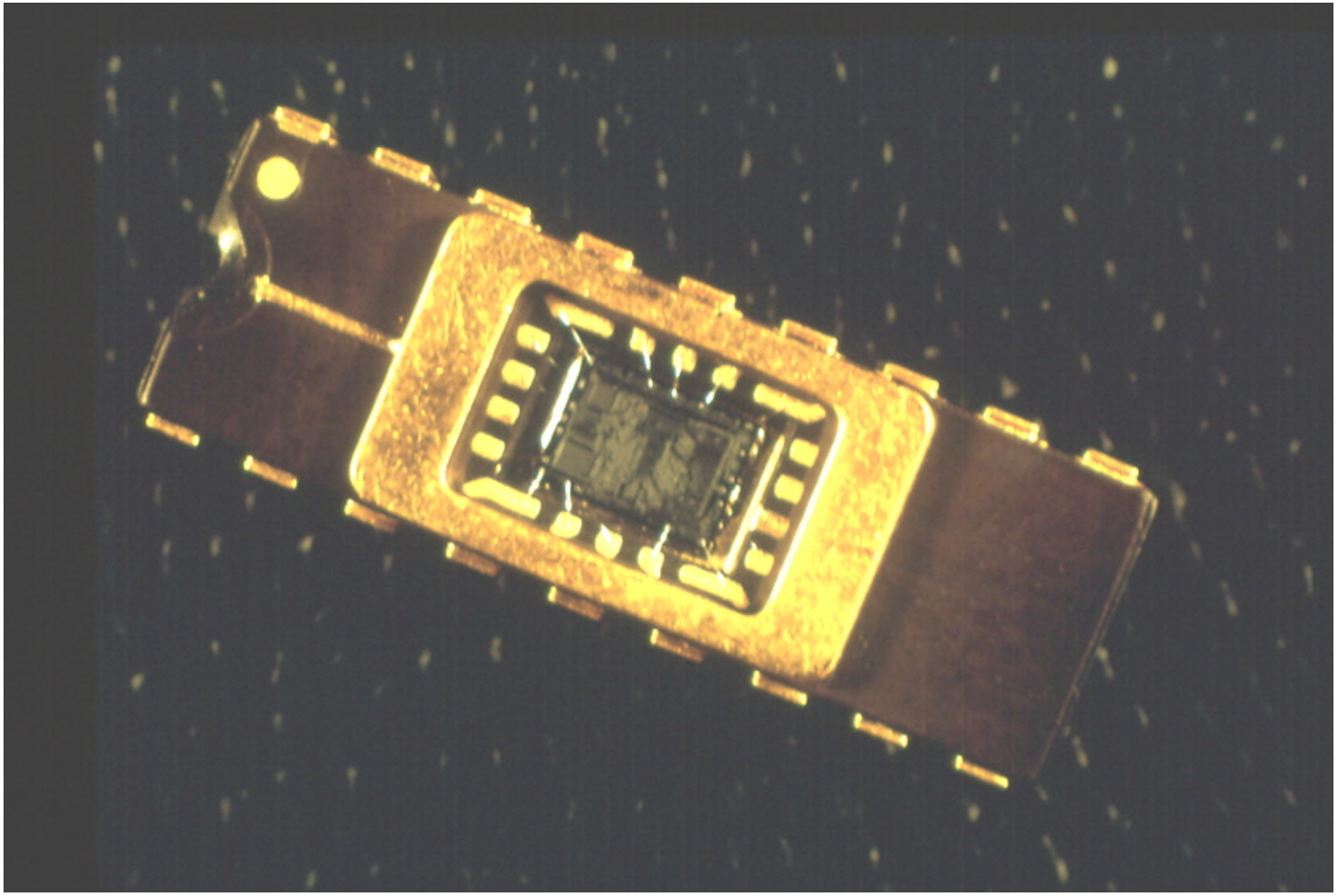


Stan Mazor in Silicon Valley: 1964 (Age 23)

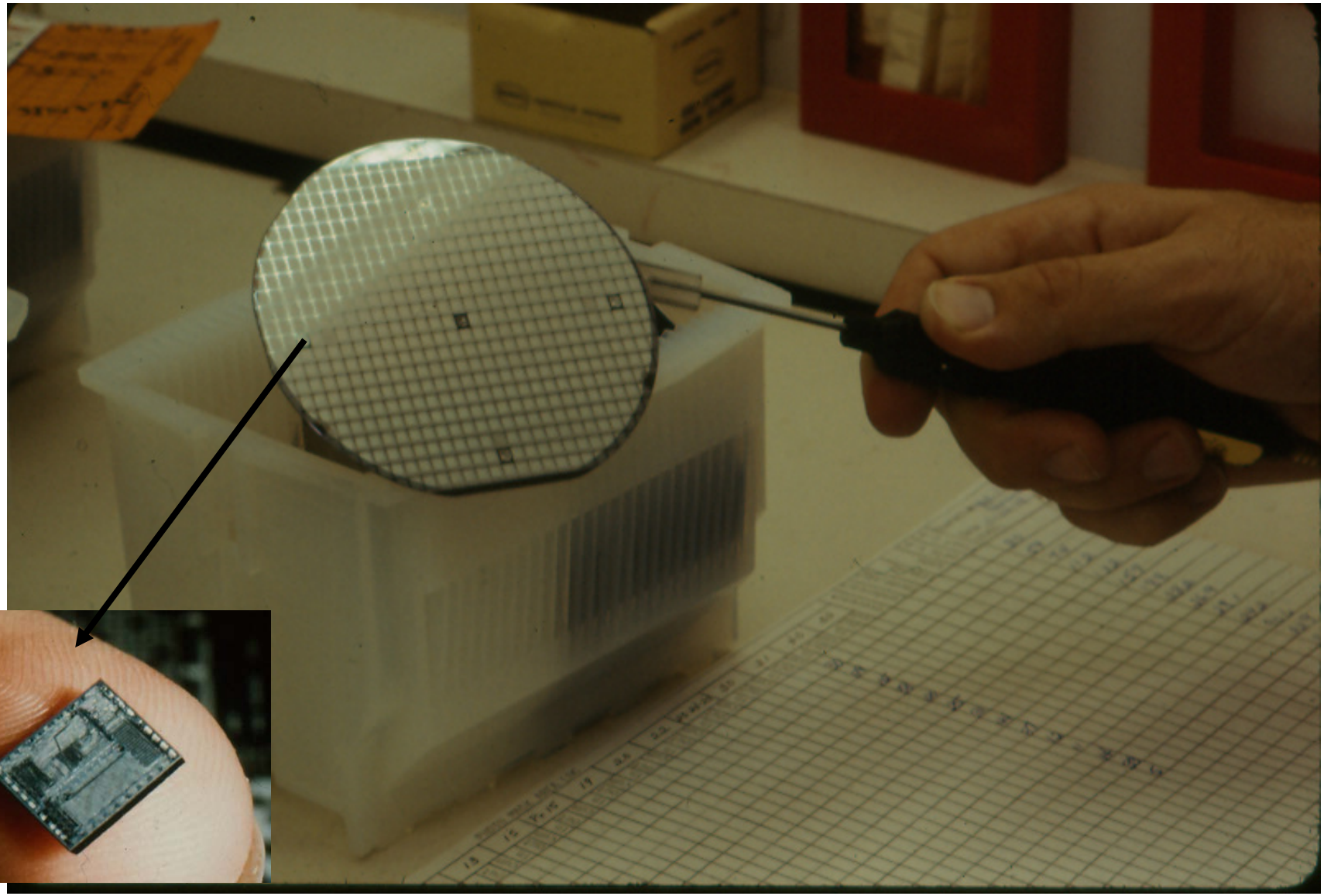
Dual Inline Packages (DIP)



Chip in Package



Silicon Wafer

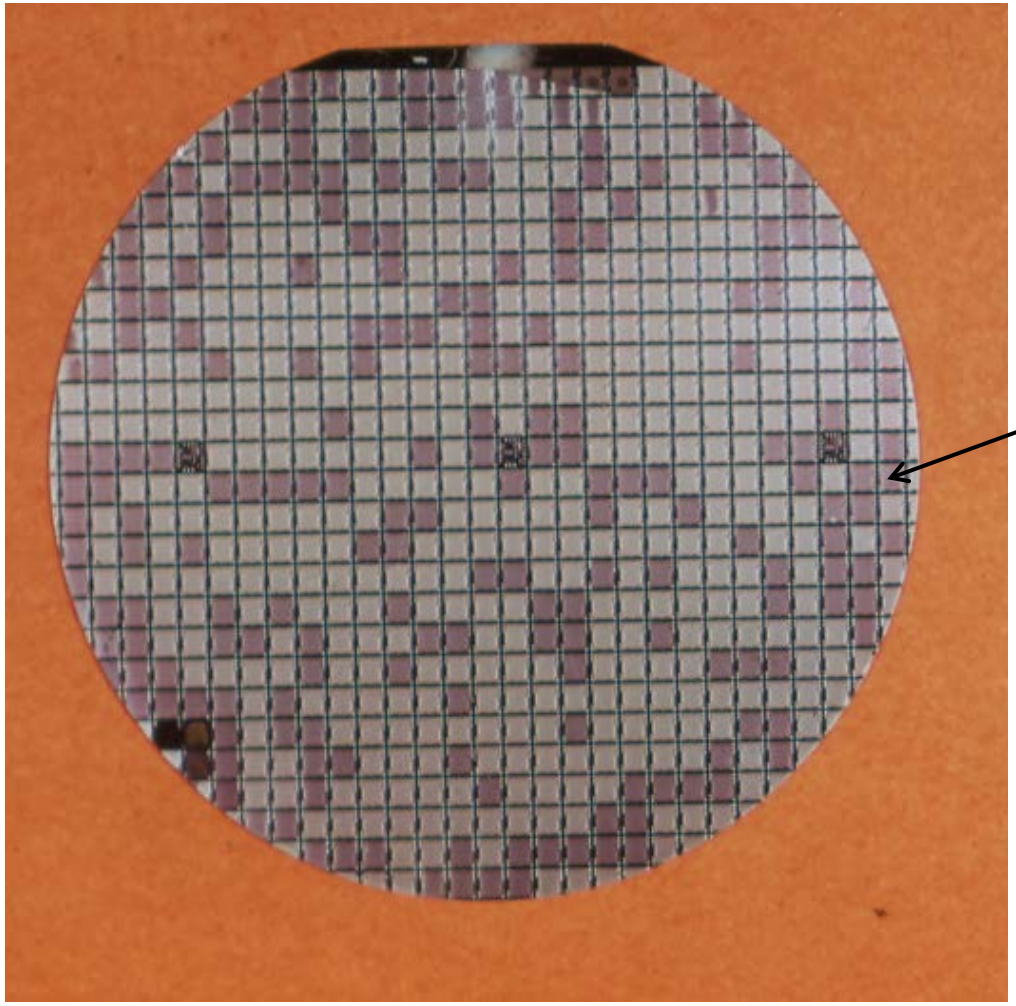


Integrated Circuit (IC) Chip

- Collection of connected transistors
  - Hoerni's "planar" process 1960
  - **Noyce** (Fairchild) CT**u**L (micro logic)
  - **Kilby** (TI) **TTL** Nobel Prize (2000)

- Limits (1970):
  - Design and layout complexity (no CAD)
  - On chip wiring (1 metal layer)
  - Package pins 14 (then 16)
  - Power dissipation (< 1 Watt)

Sorted Wafer



300 + processing steps

20+ photographic steps

~3 months to make

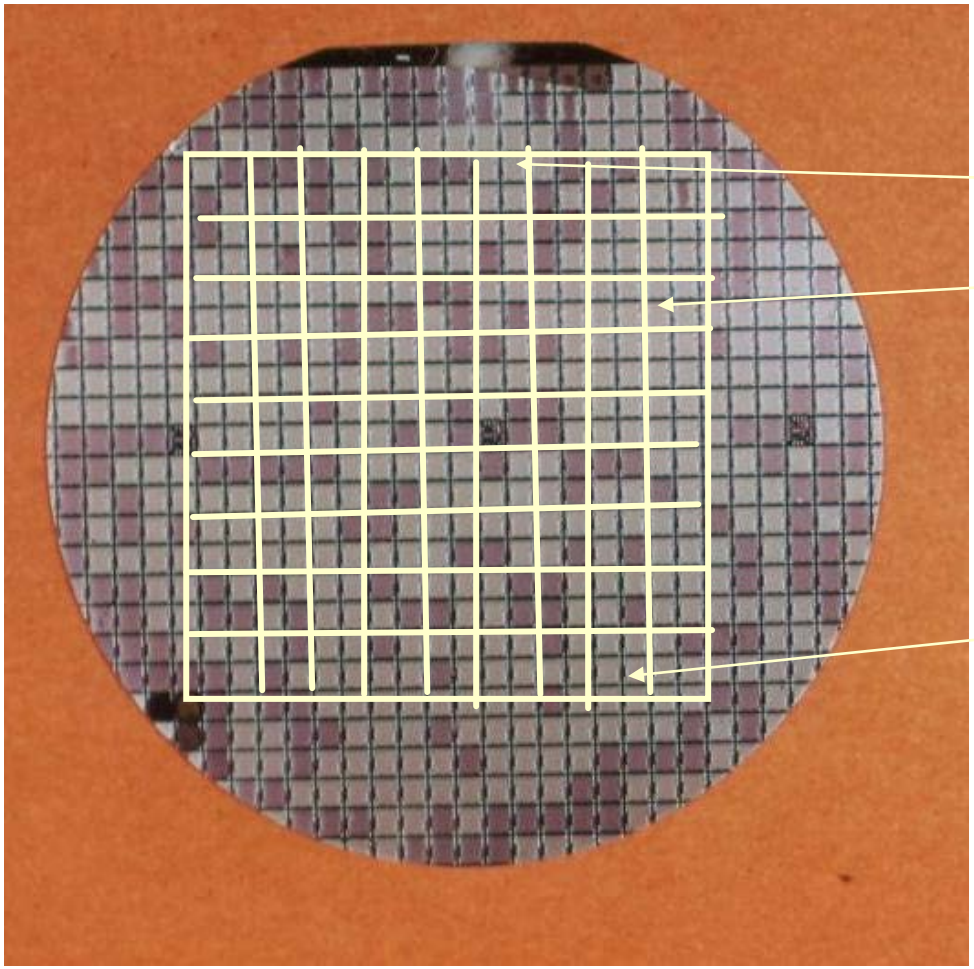
Ink marks defective dice

Defects:

- wafer material defects
- processing defects
- statistical limits

Yield Estimate: 4X Larger Die

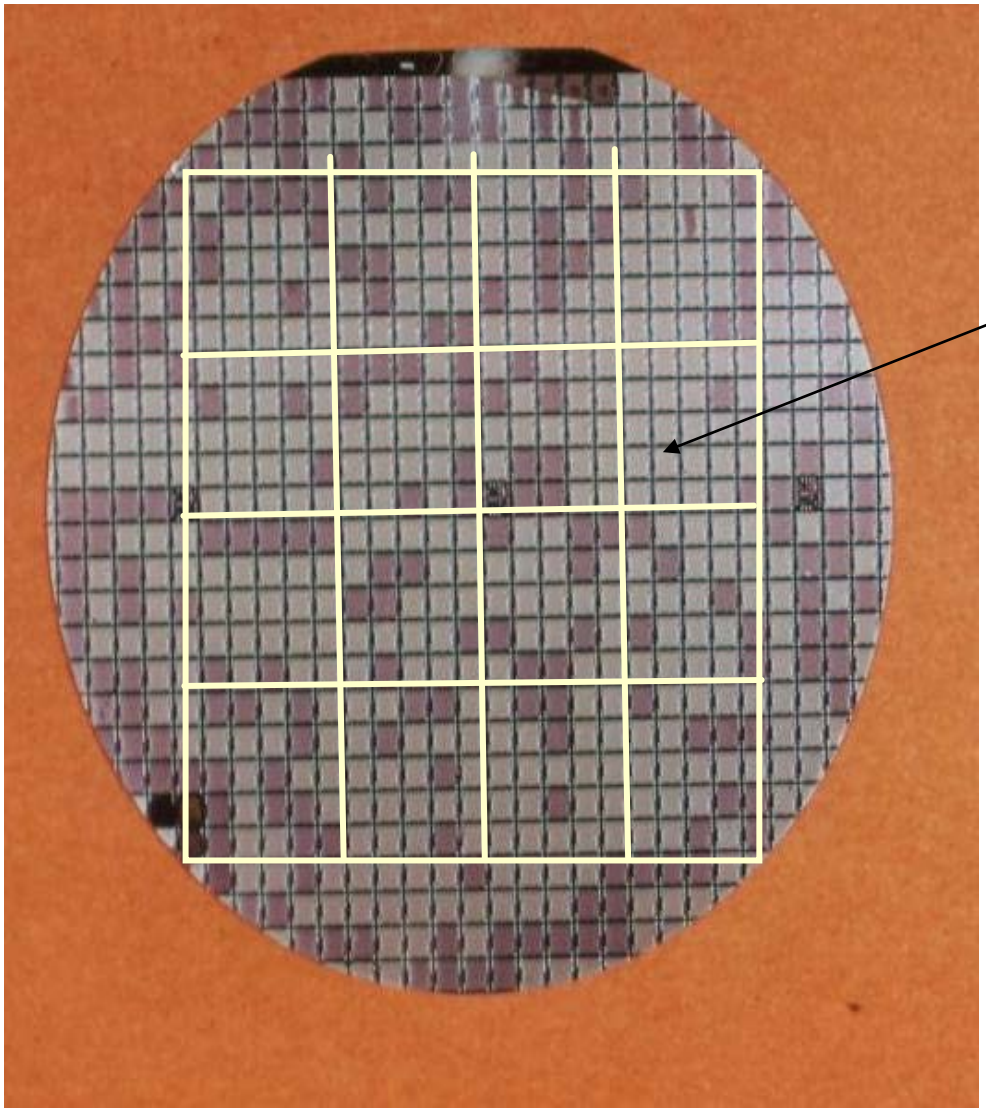
Bigger Chip = Lots of stuff Few good ones



1
3
5
3
4
1
3
2
3
25
(of **81**+ possible)

Yield 25/81 = **30%**

Yield Estimate: 25X Larger Die



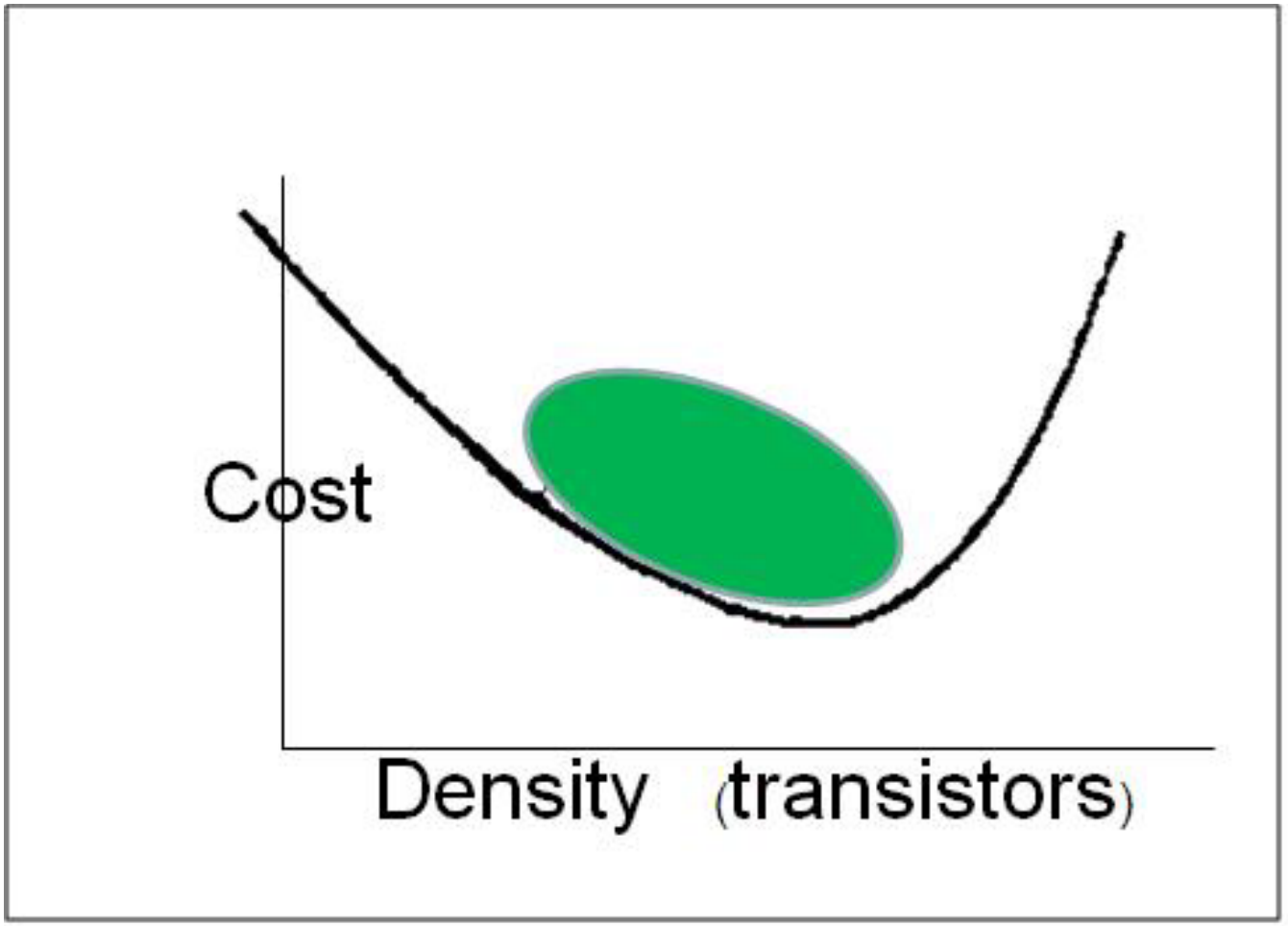
Almost 1 good (of 16 possible)

Zero Yield

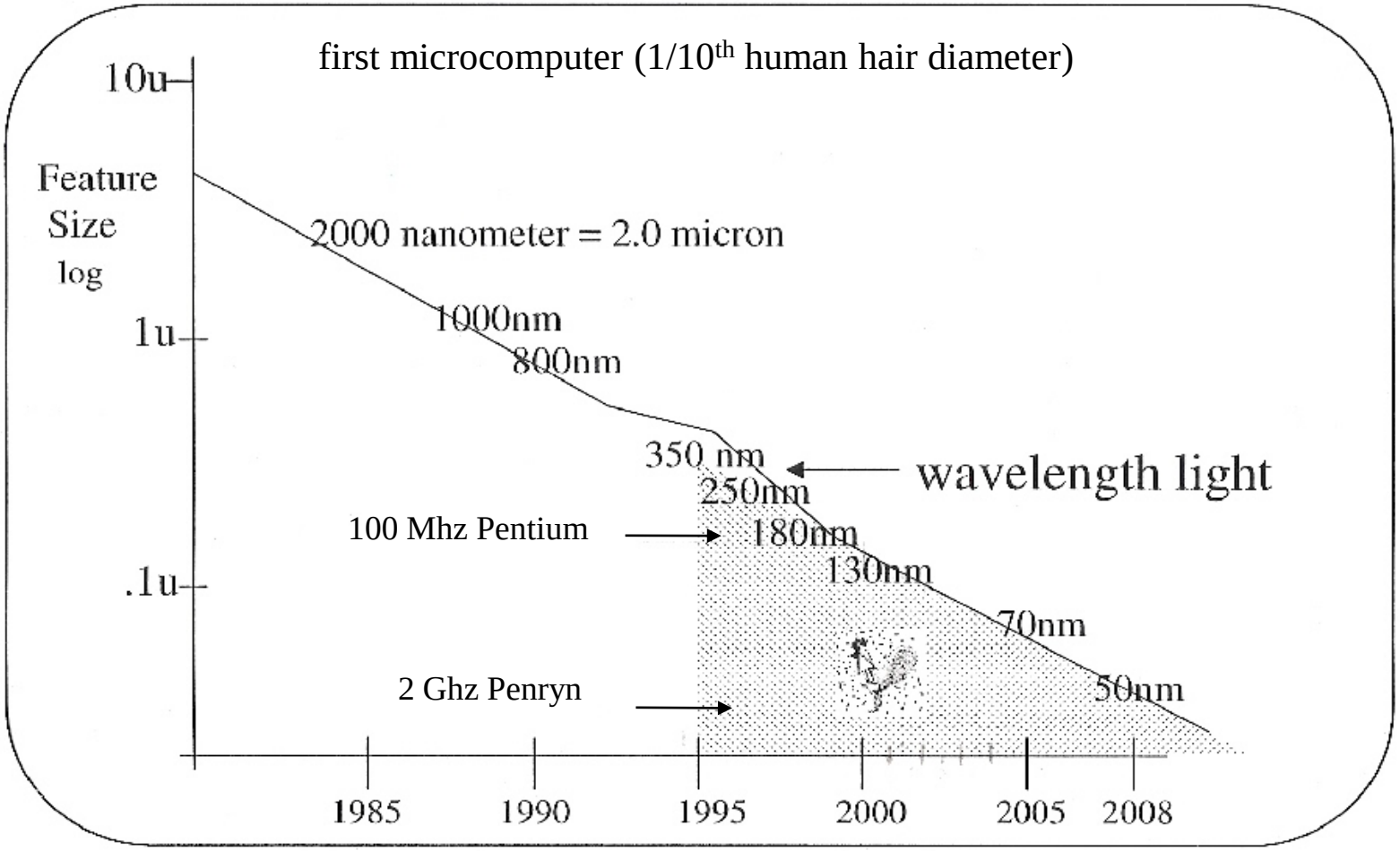
Big Chips = Lots of stuff

No good chips

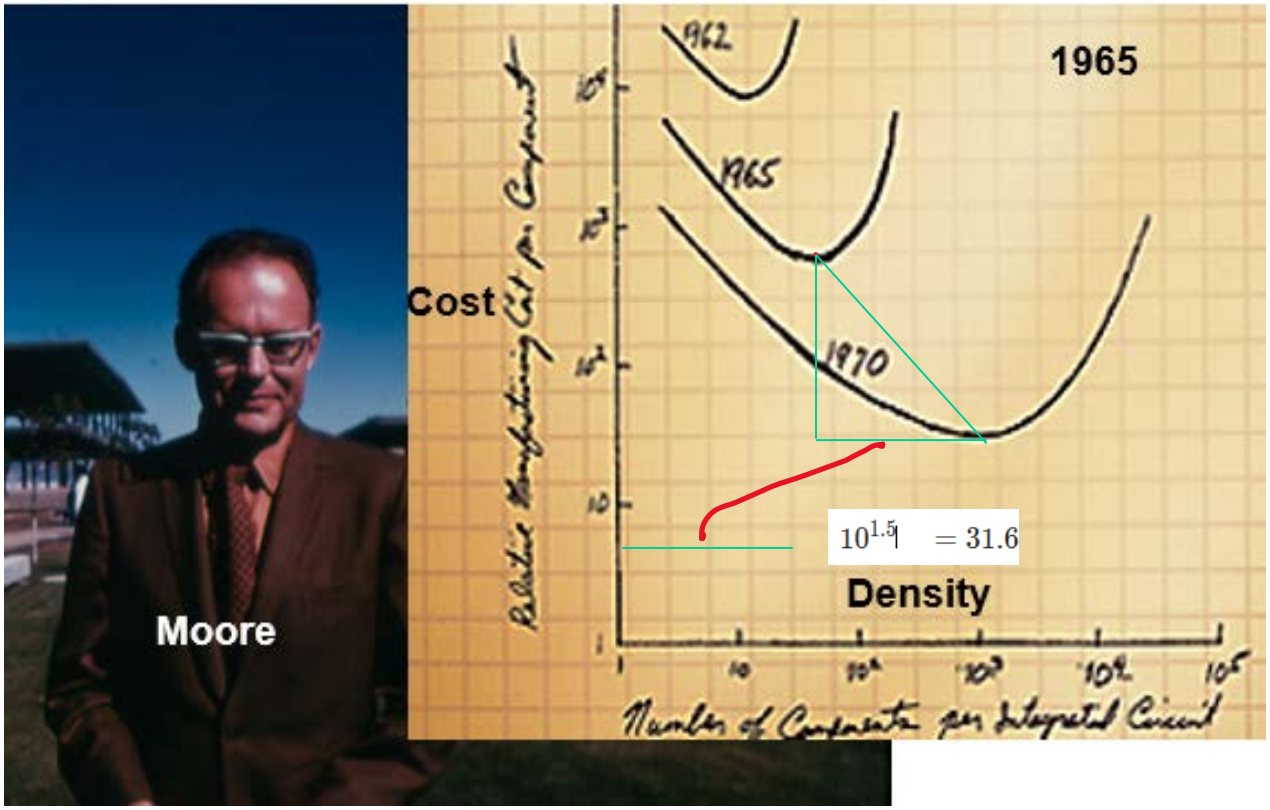
Transistor Cost v. Density: Bathtub Curve



Chip Object Sizes



Gordon Moore's 1965 Observation at Fairchild (aka, "Moore's Law")

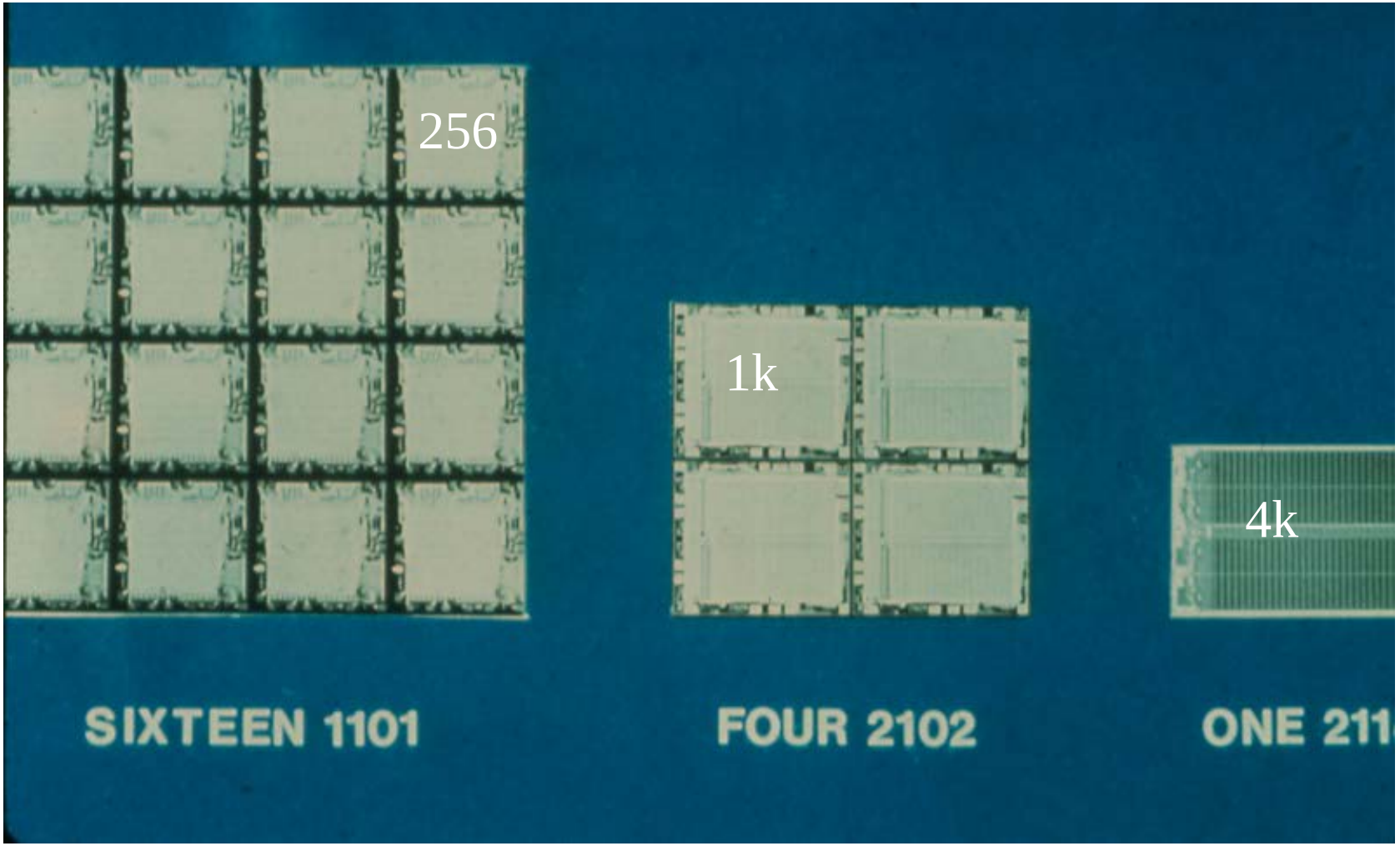


- Select chip Cost
- Density increase

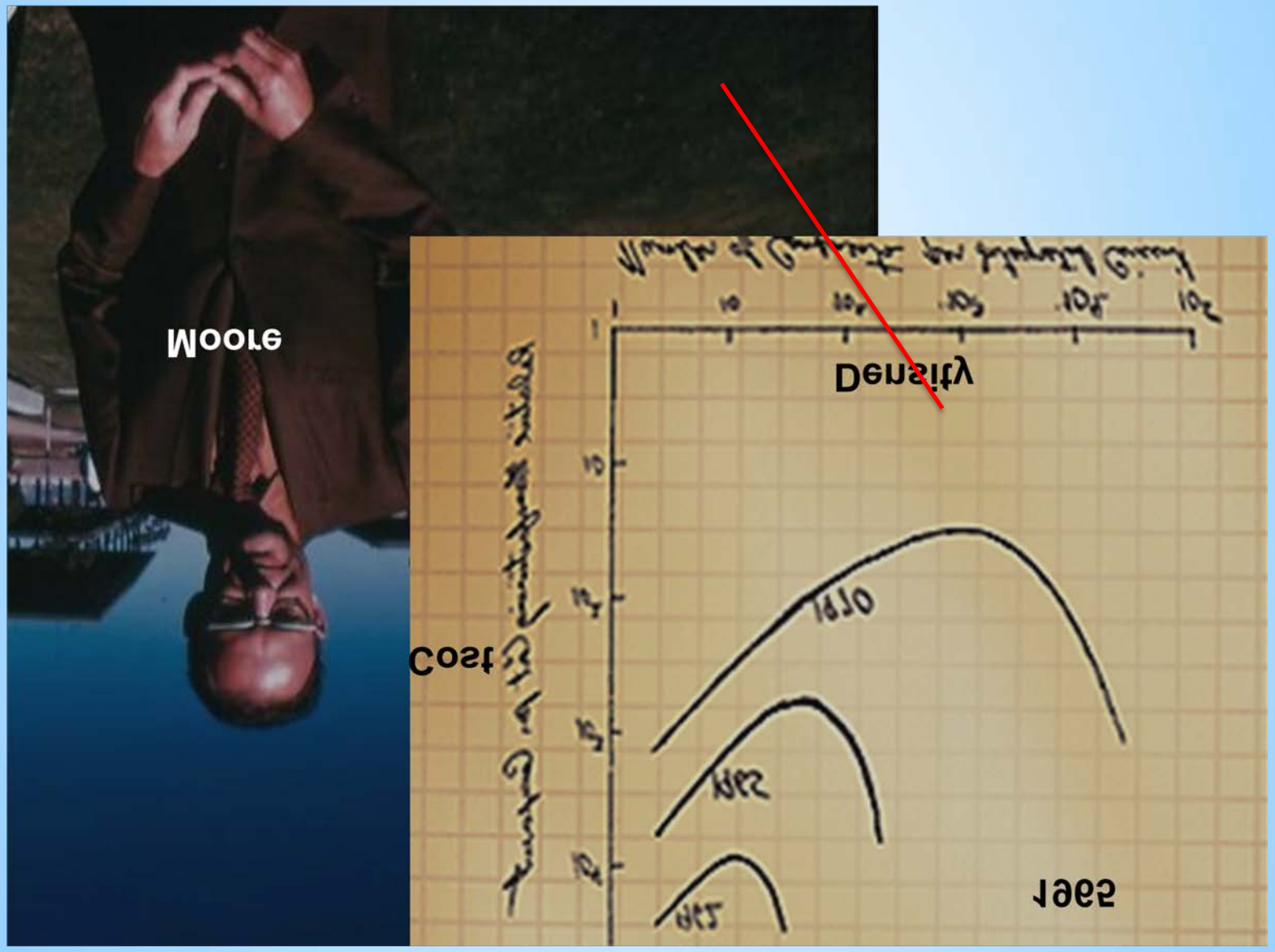
  ~32x in 5 years

  Doubles yearly

4k Bits Static RAM (chips)

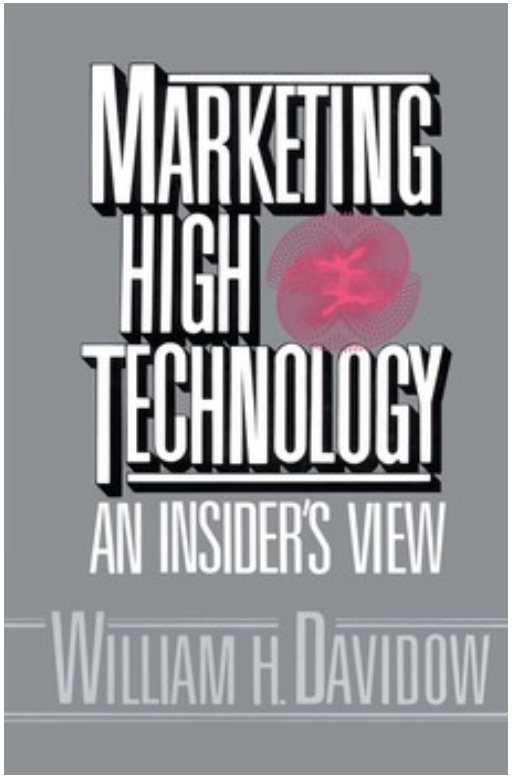


Another View of Moore's Law



Reflections on Gordon Moore by Bill Davidow of Mohr Davidow Ventures

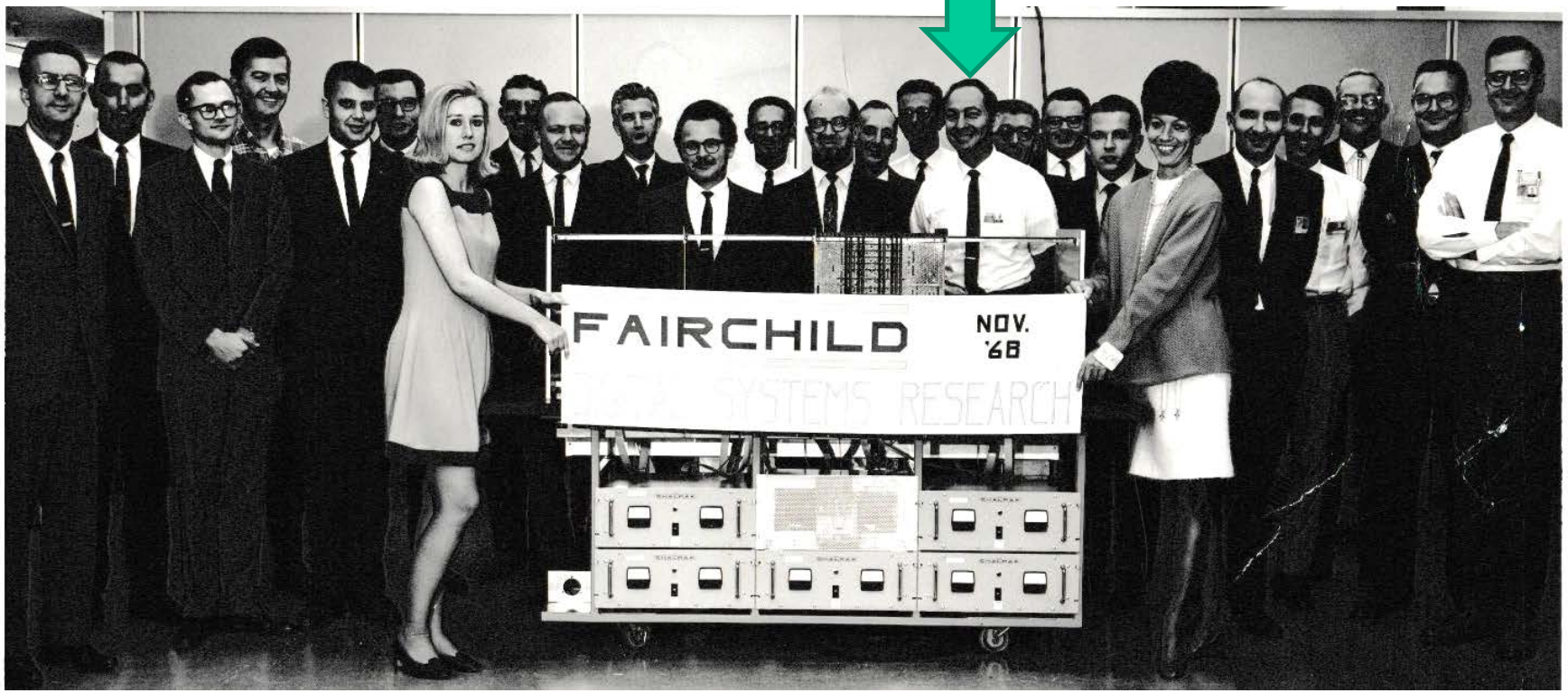
MOHR DAVIDOW VENTURES



Gordon Moore's Fairchild R&D Projects (1966)

- Micro Mosaic: standard cells
- Micro Matrix: gate arrays
- Fairsim: logic simulator and CAD tools
- **Symbol:** large scale computer
- Op Amp: analog circuit

Fairchild Symbol 2R Computer Intro (1968)



Use 10x more logic
Plan for future LSI
20 guys for 5 years

Fairchild Symbol Computer

Stanley Mazor
IEEE, Sr. Member

IEEE Annals of the History of Computing story by Stan (Jan-March 2008)

Features of the Symbol computer:

- New Symbol programming language
- Hardware directly executed Symbol source code
- Compiler and operating system built with hardware
- Memory controller provided virtual memory
  - US Patent 3,647,348 (Stan was co-inventor)
- Hardware supported dynamically-varying sized data

Printed Circuit Board (PCB)

Printed wires

200 IC’s

Symbol Program Example

Y = “is good”;

Y = “ is much better than it was”;

Y = 3/2;

Y[2] = <18, 24,36>;

Memory Operations

- *Assign group—AG*. This operation allocated a new group from the storage free list, (allocated a new page if needed), and returned the address of the first word in the group.
- *Store and assign—SA*. This operation stored the data word at the address sent, and returned the next sequential address for the following word in the same group. If the group was full, it allocated another group from the free space pool, and linked the groups together, and returned the address of the next free location in the group.
- *Fetch and follow—FF*. This operation fetched the data word at the address given and returned the next sequential address of data, if in another group, it followed the link. If this was the end, it returned a null address.

Integrated Circuit (IC)

- Limits (1970):
  - Design and layout **complexity** (weak CAD)
  - On chip **wiring** (1 metal layer)
  - Package **pins** 14 (then 16)
  - **Power** dissipation (< 1 Watt)
  - Logic gates and 4-bit latch

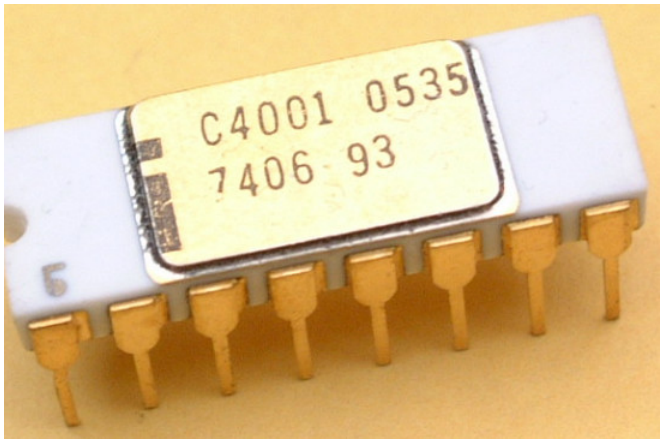
1969: Move from Fairchild to Intel

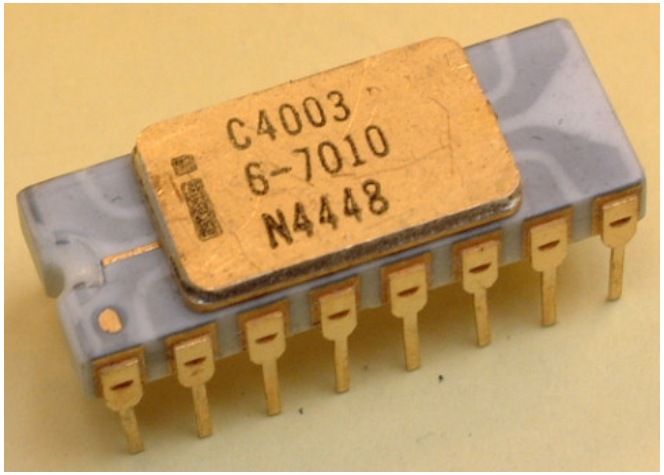
FAIRCHILD SEMICONDUCTOR®

intel

MCS-4 (My Memories)

- ROM memory 4001
- RAM memory 4002
- Shift register (memory chip) 4003

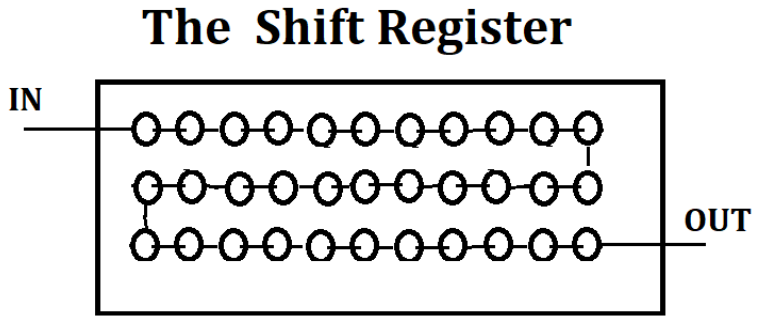




Glass Teletype (1970)

- Competitive cost vs teletype
- Beehive, Wyle, Hazeltine, **Datapoint**
- Memory data: 25 lines x 80 char/line
  Serial 2,000 chars x 6 bits = **12k** bits
- **Shift register** memory chips
- Datapoint 2200 8-bit computer
- Intel **8008** CPU chip (patents)

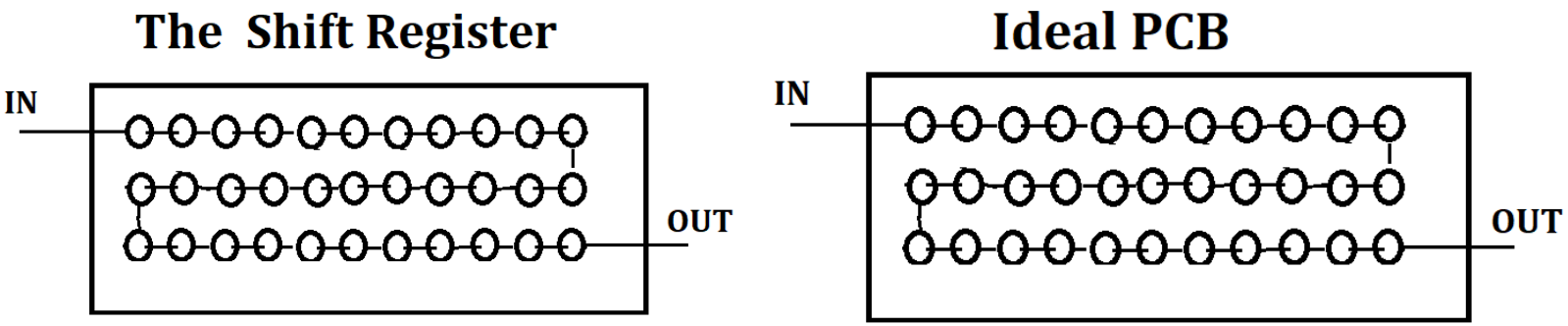
Ideal Memory Chip



- 1k bits ‘same’ cell layout
- Short wires connect neighbors
- 2 data pins IN and OUT

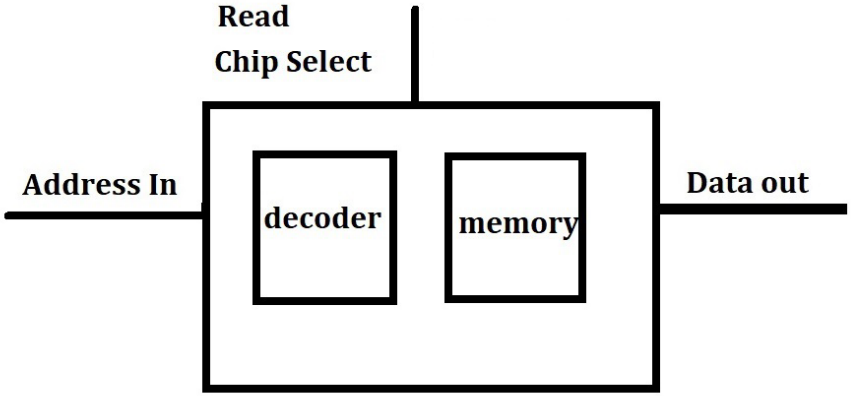
Ideal Memory Chip Layout (S)

Ideal Memory Chip and PCB



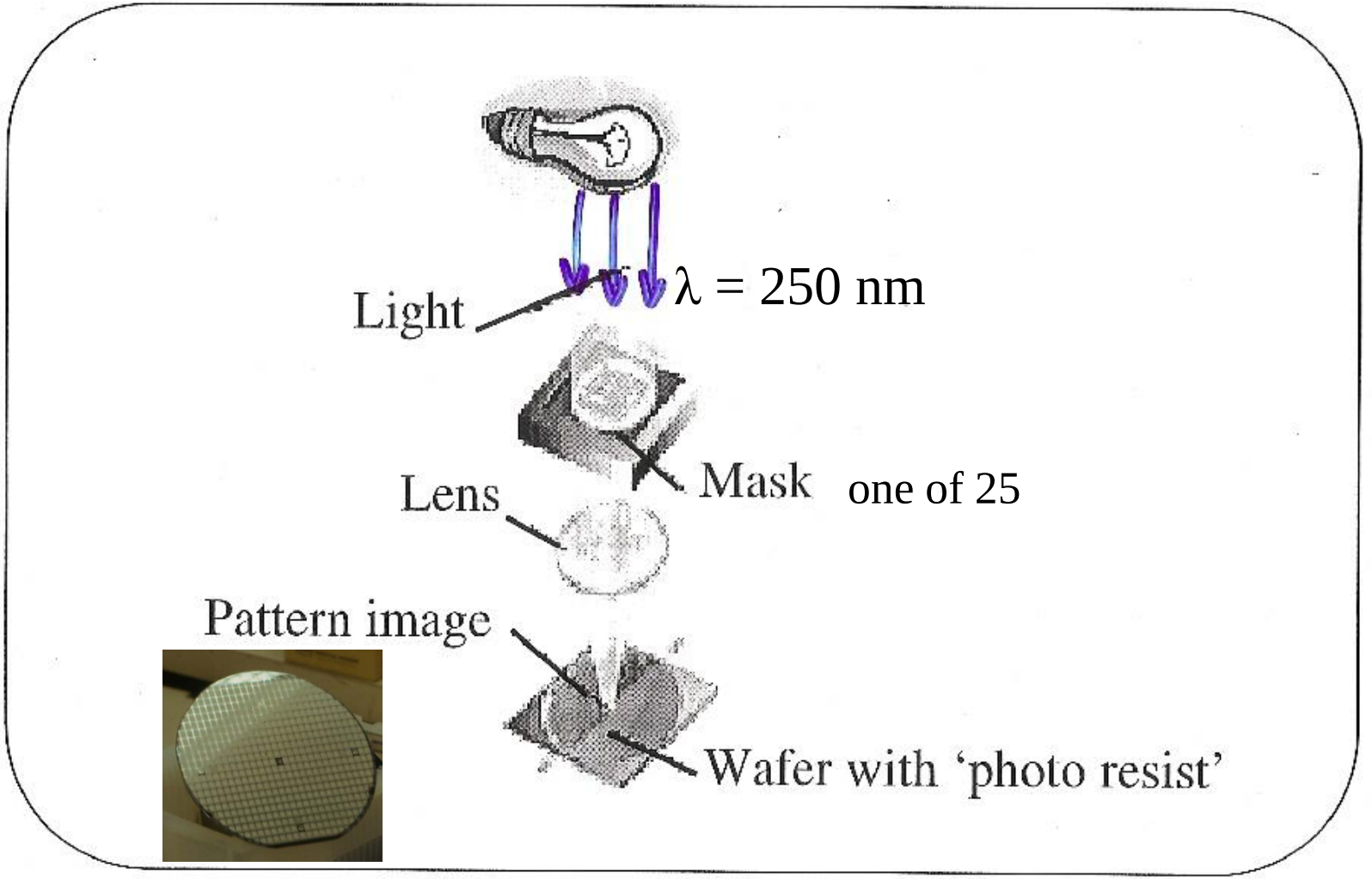
- All chips are 1k SR's
- Short wires connect neighbors
- 2 data pins IN and OUT

Random Access Read Only Memory (ROM)

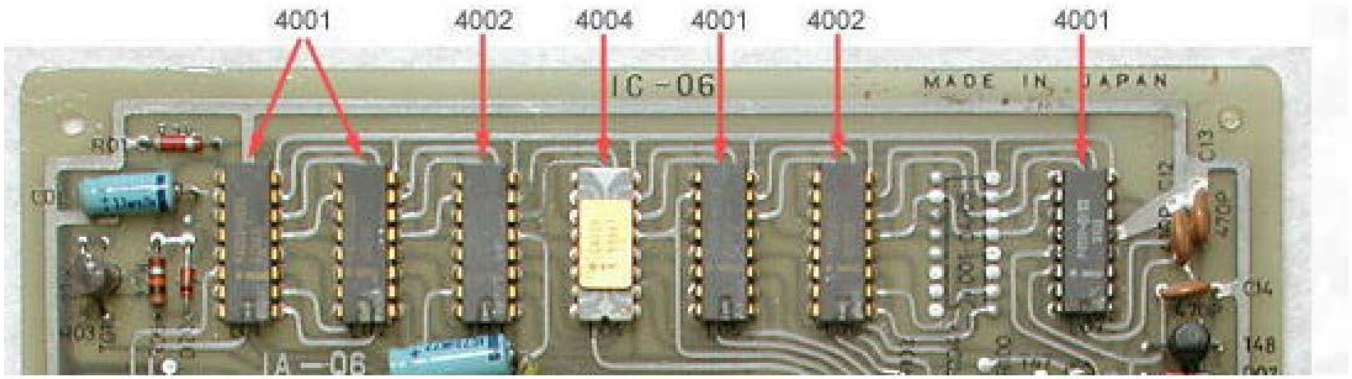


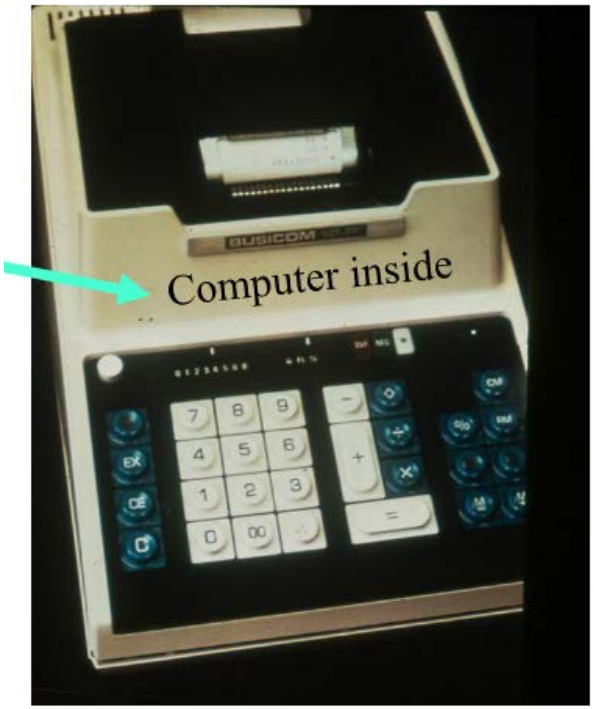
- Layout Mask sets (writes) data
- Random access (Address In) selects data
- **Chip Select** enables Data **out**

Photo Lithography



Busicom Calculator MCS-4 Chips

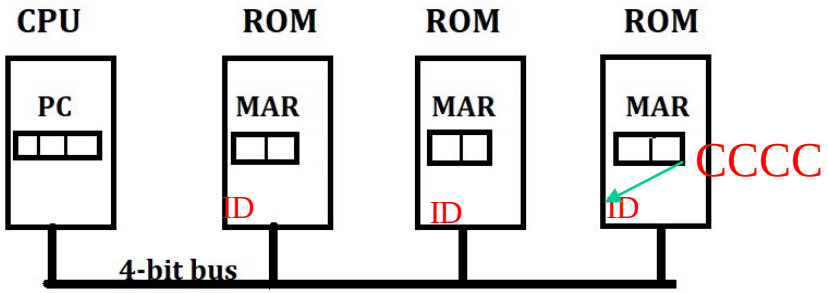




CPU Acc, 16 index regs, 4-bit, 45 instr. 4004
4 ROM 256 x 8 = 1k program code 4001
2 RAM 4 register x 16 digit x = 8 numbers 4002
Serial 14 digit floating point arithmetic
Need I/O signals for keyboard and printer
6 memory chips x **4 pins** = 24 I/O pins
15 V PMOS SiGate

Pins are valuable, logic is cheap

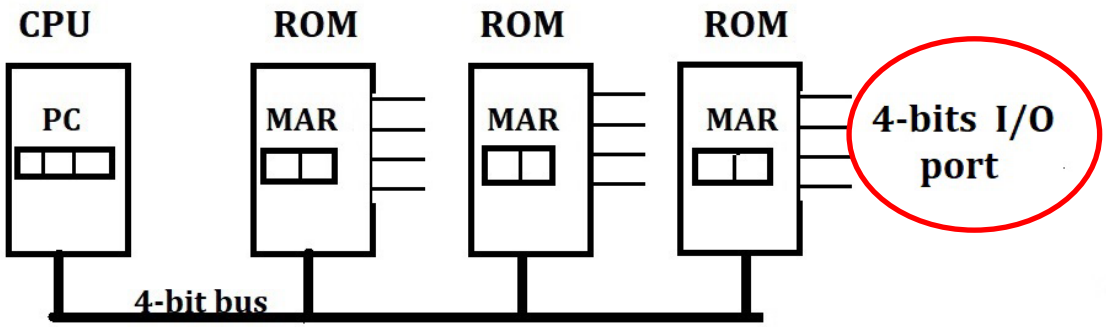
CPU (4004) / ROM (4001)

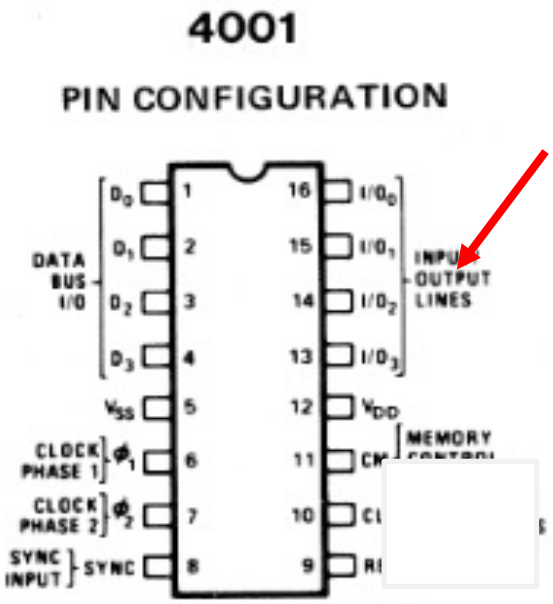


Sent last

12- bit Program Counter **PC (**CCCC HHHH LLLL**)**
8- Memory Address Register **MAR** gets (LLLL, HHHH) :c1, c2
ROM 256 x 8 ; 8 bits read (every ROM) using MAR :c3
ROM has 4-bit ID code CCCC
CPU sends chip ID CCCC to all ROM's :c3
The **selected** ROM sends 8-bits (op code) to CPU :c4, c5
No Chip Select (CS pin) on ROM (CCCC selects one ROM ID)

4001 ROM: 4-bit I/O port



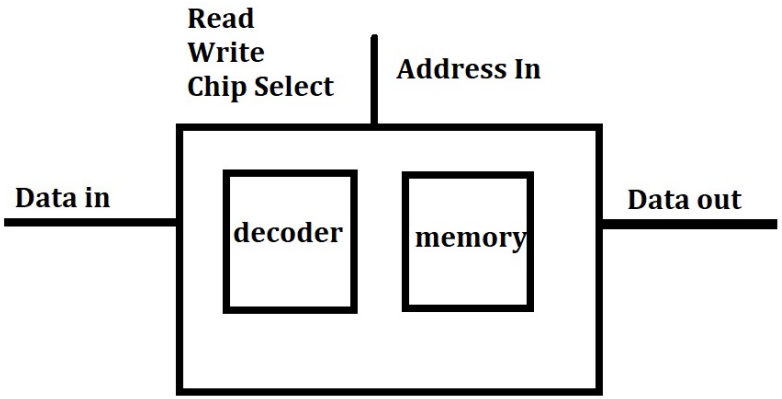


Each 4001 ROM has 4 bit I/O port (pins)
CPU executes Read/Write of ROM port
ROM sees/decodes op code :c4, c5 (**no control pins)**
CPU op: **RDR** reads ROM port 4-bits into ACC
CPU op: **SRC** selects a ROM chip port (previously)

IBM Core Memory Unit

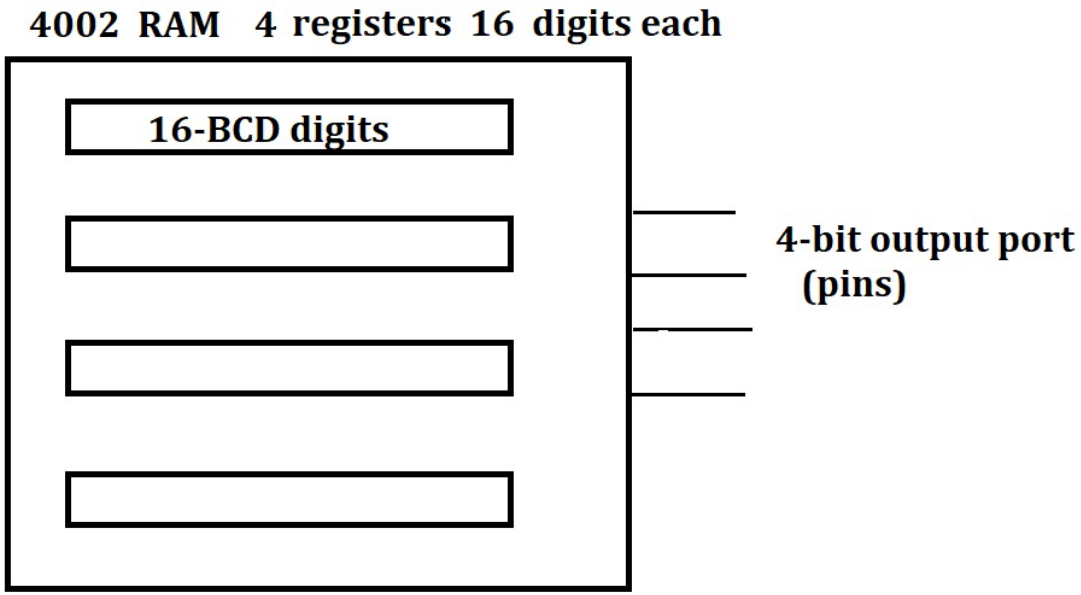
- Extends Main Frame memory
- Read/Write memory ops (transparent)

Random Access Memory (DRAM)



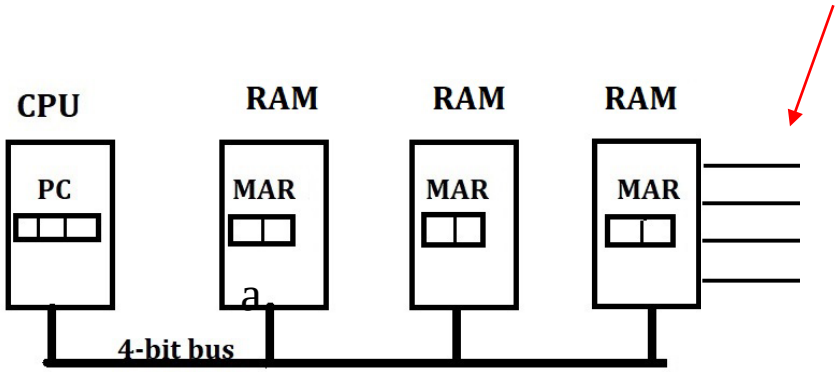
- Random access (Address In) selects data
- Data **in** and Data **out**
- **Read** out or **Write** data in

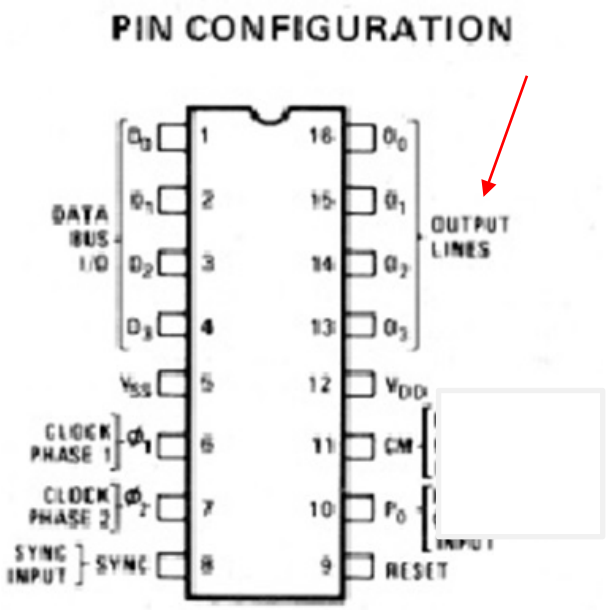
4002 RAM: 4 Registers



- RAM ID is 0-3 **built-in**

4002 RAM





Read/Write RAM data (Data in, Data out)

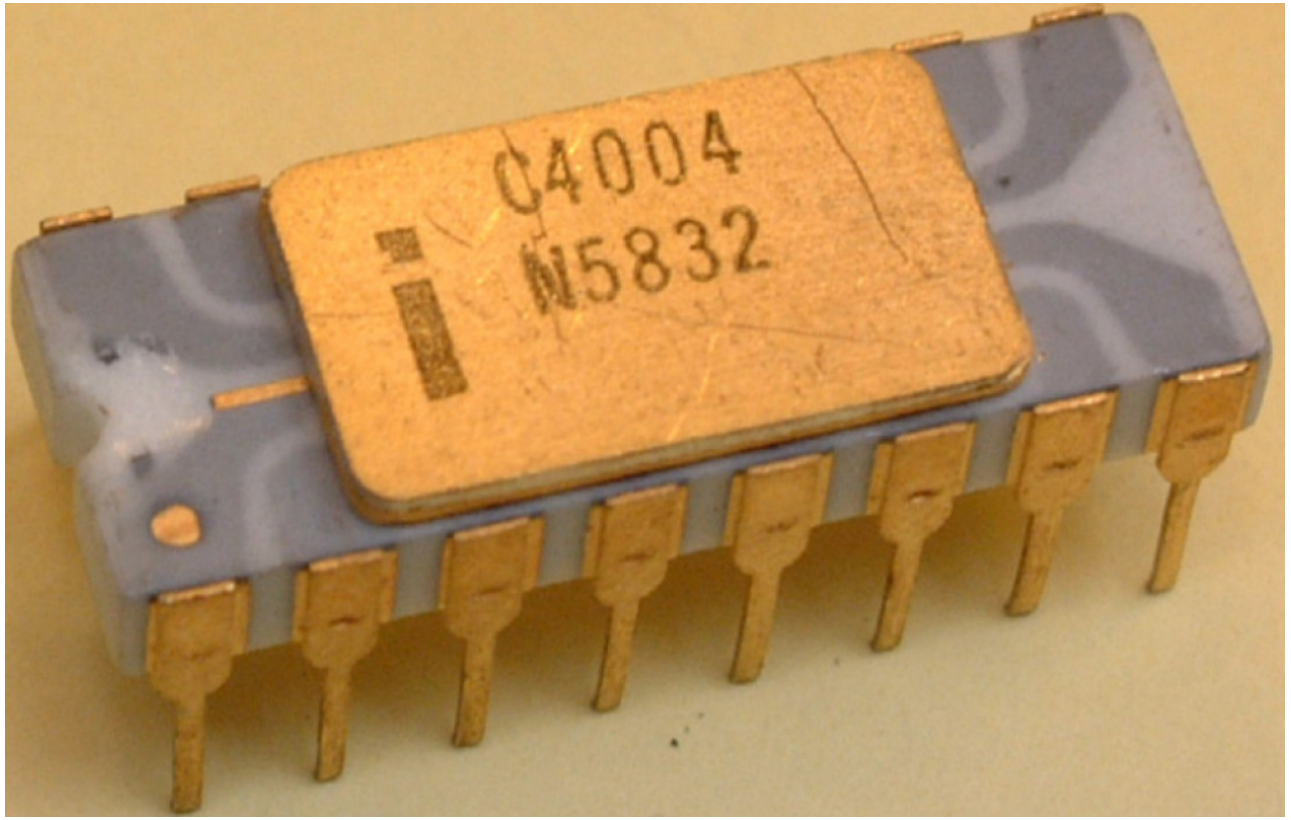
No Read or Write pin on 4002 RAM

Write ACC to 4- bit port

No Write port pin on 4002 RAM

4004 CPU Read Port Instructions

E9	RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator
EA	RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator (I/O Lines)



8008 Microprocessor Spec

CTC CPU PRELIMINARY DESCRIPTION

THE CPU IS AN 8 BIT PARALLEL CENTRAL PROCESSOR UNIT FOR A COMPUTER SYSTEM. IT CAN BE INTERFACED WITH VARIOUS MEMORIES HAVING CAPACITIES UP TO 16K BYTES.

THE PROCESSOR COMMUNICATES OVER AN 8 BIT DATA & ADDRESS BUS AND USES 2 INPUT AND 2 OUTPUT LEADS FOR CONTROL. TIME MULTIPLEXING OF THE DATA BUS ALLOWS CONTROL INFORMATION, 14 BIT ADDRESSES AND DATA TO BE TRANSMITTED BETWEEN THE CPU AND MEMORY.

THE CPU CONTAINS TEN 8 - BIT DATA REGISTERS AND A 14 - BIT PROGRAM COUNTER. AN 8 - BIT PARALLEL BINARY ADDER - SUBTRACTOR IMPLEMENTS ARITHMETIC & LOGICAL OPERATIONS. A MEMORY STACK CONTAINING SEVEN 14 - BIT WORDS IS INTERNALLY USED TO STORE PROGRAM SUBROUTINE ADDRESSES.

THE CPU CONTAINS 100K TO IMPLEMENT A VARIETY OF REGISTER TRANSFER, ARITHMETIC, CONTROL AND LOGICAL INSTRUCTIONS. SOME INSTRUCTIONS ARE CODED IN ONE BYTE (8 BITS). DATA IMMEDIATE INSTRUCTION USE 2 BYTES; JUMP INSTRUCTIONS UTILIZE 3 BYTES. OPERATING BETWEEN 1 & 2 MICROSECOND CYCLE TIME THE CPU EXECUTES NON MEMORY REFERENCING INSTRUCTIONS IN UNDER 10 MICROSECONDS.

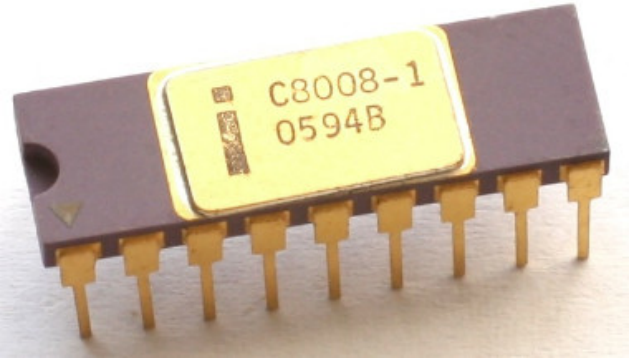
jm 3/4/70

Written @ Intel 1971

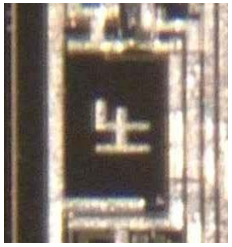
Design issues:

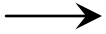
- **die size**
- **power dissipation**
- **package pin count**
- **testability**

Patented by TI



8008 Microprocessor: 1972





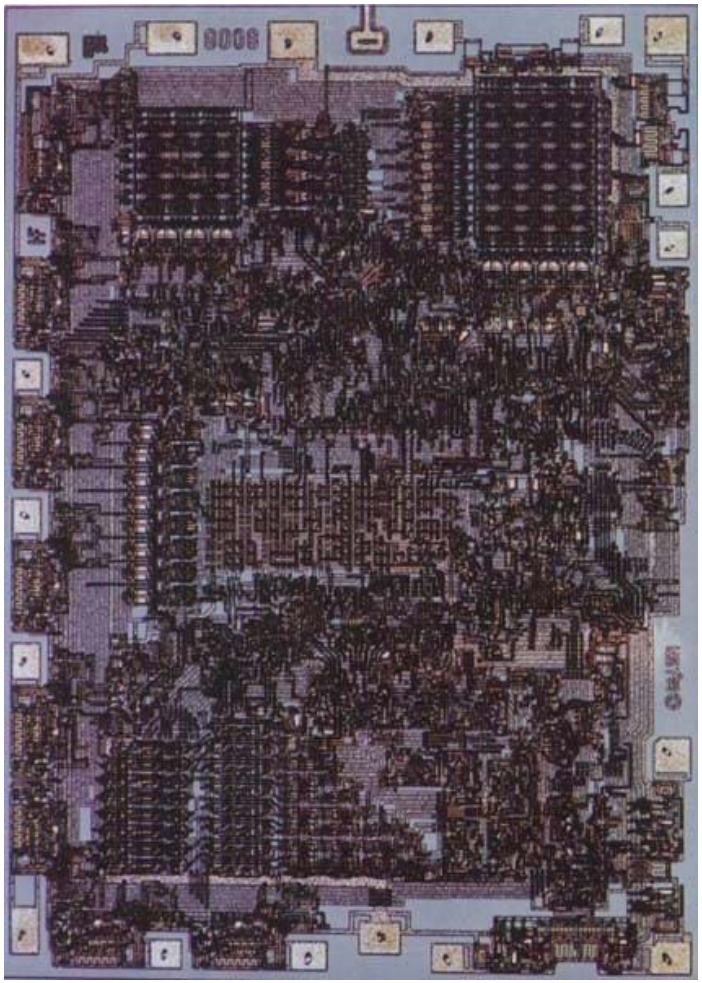
Hal **F**eeney
designer

18 pin package

14 volts

1/2 Watt

124 x 173



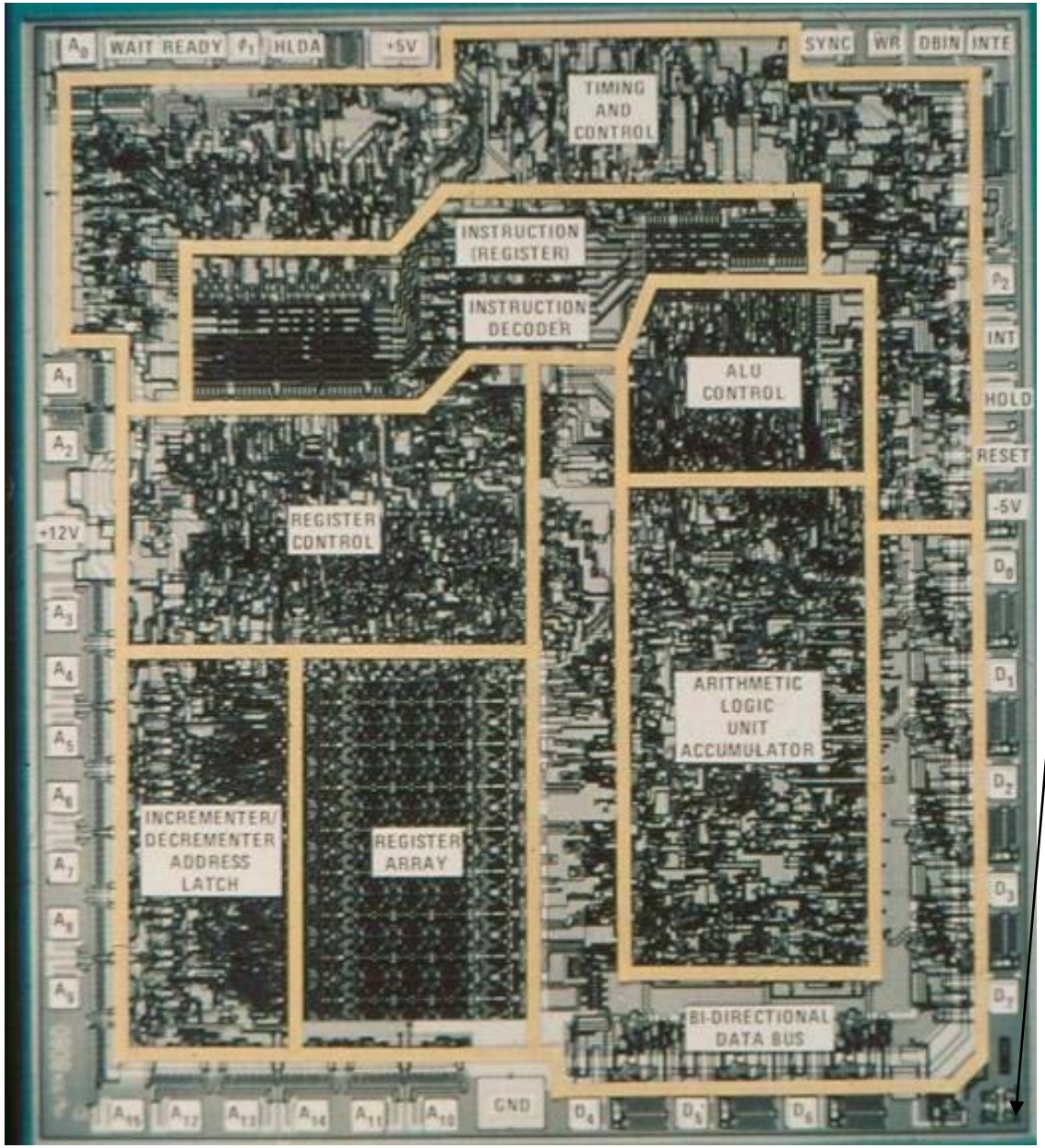
Registers: 7 x 8-bits

PC Stack: 8 x 14-bits

Instruction Decoder

8-bit ALU

Intel 8080 Chip: 1974



40- pin DIP

5 Volts

3/4 Watt

M. Shima (island)

Intel Microprocessor Credits

4004 Microprocessor (1971)

- **Hoff**: MCS-4 architecture and instruction set (before Stan joined)
- **Mazor**: added 4 instr. (FIN, JIN, +2); wrote interpreter and code
- **Faggin**: did all logic, circuit design, layout, testing, and chip plans
  - (1974 Intel patent: US 3,821,715)
- **Shima**: Busicom calculator designer: all coding, assisted layout verification

8008 Microprocessor (1972)

- **Mazor**: proposed 8-bit CPU
- **Faggin**: supervised (**Feeney**) (1973 TI patent: US 3,757,306)

8080 Microprocessor (1974)

- **Faggin**, **Shima**, **Mazor** (1977 Intel patent: US 4,010,449)

Conclusions

- Known physical limits may be overcome (maybe not)
  - Moore's law will slow down
  - Chip heat and energy issues prevail
- Technology requires large financial investment
  - Invest only if there is a market
  - New technologies enable new markets
- Existing approaches tend to saturate
- Some new directions identified, but are unproven

Patents

Fairchild awarded US Patent No. 3,647,348 on March 7, 1972 for
Paging system supporting Virtual Memory (**Symbol Computer**)
“Hardware-Oriented Paging Control System”
William Smith, Rex Rice and Stan Mazor 2 Claims: transfer of pages

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Intel awarded US Patent 3,821,715 on June 28, 1974 for
3-chip computer with single chip **4-bit** CPU **(4004)**
"Memory system for a multi-chip digital computer,"
Ted Hoff, Stan Mazor, Federico Faggin 17 Claims: memory schemes

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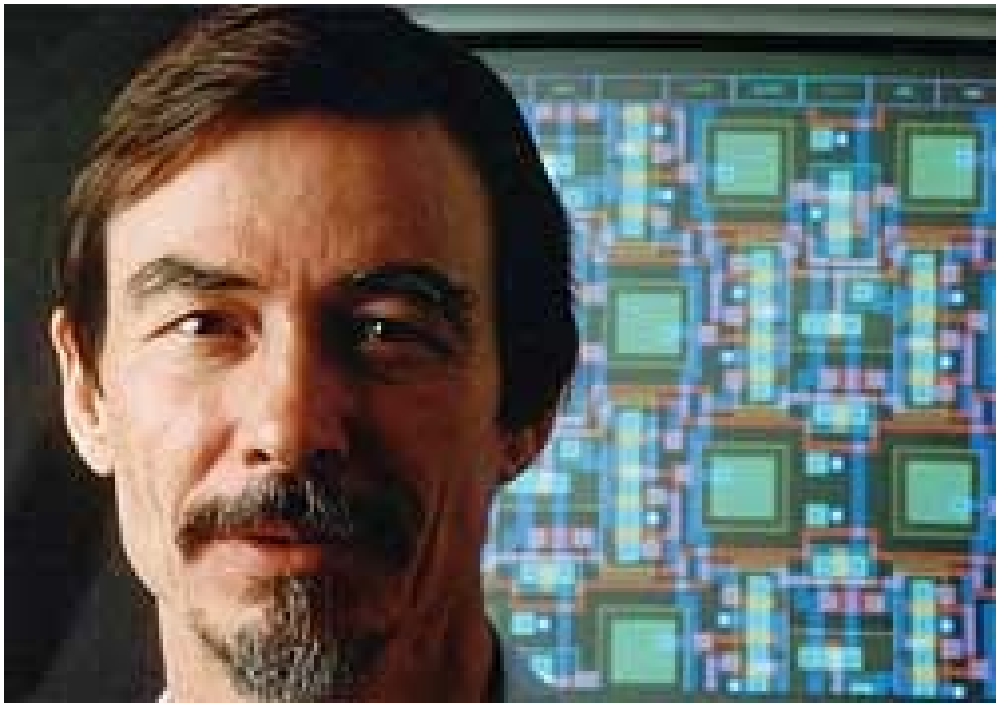
TI awarded US Patent 3,757,306 on September 4, 1973
for the single-chip **8-bit** CPU (**8008**) 8 Claims: CPU

Intel awarded US Patent 4,010,449 on March 1, 1977 for
"MOS Computer" (**8080**)
Federico Faggin, M. Shima, Stan Mazor 2 Claims: coding

1983: Silicon Compilers

- Founded in 1981 by Carver Mead, David L. Johannsen, and Edmund K. Cheng



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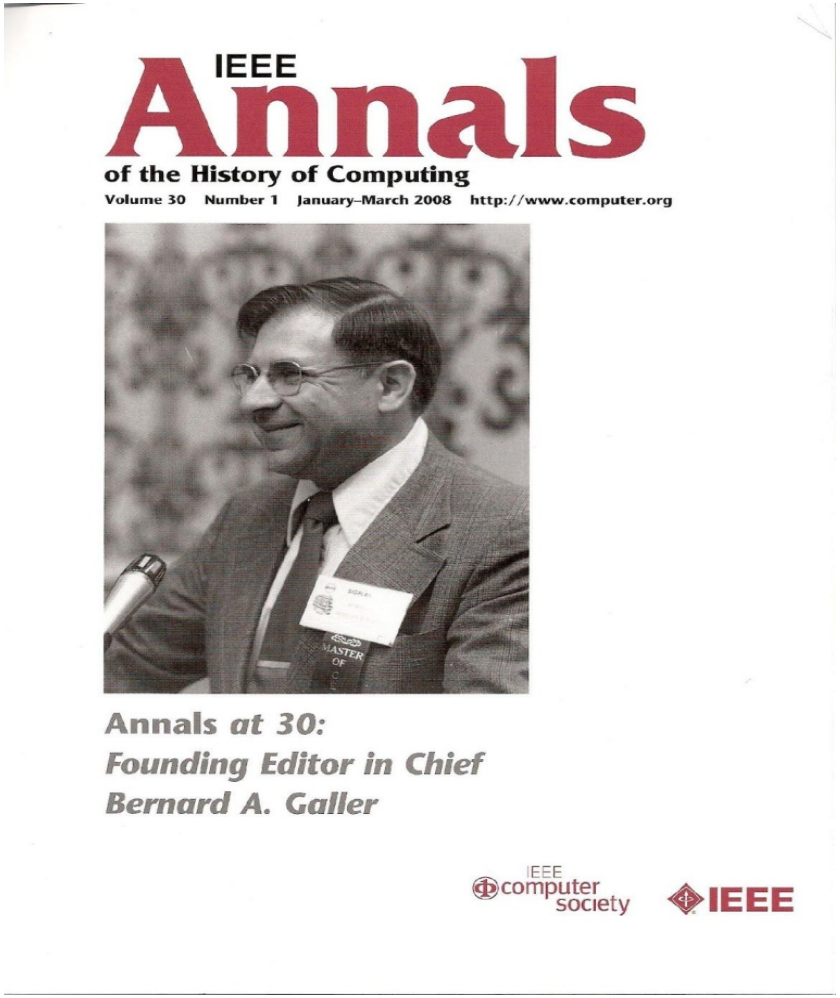

Mazor's writings:

- **Intel 4004: 2005**
- **Intel 8008: 2006**
- **Intel 8080: 2007**
- **Symbol Computer: 2008**
- **Magnavox video game: 2009**
- **Intel 8086: 2010**

Recognitions

- 1996: National Inventors Hall of Fame
- 1997: Kyoto Prize
- 2000: Robert N. Noyce Award
- 2009: Computer History Museum Fellow
- 2009: National Medal of Technology and Innovation
  - From Pres. Obama, with Ted Hoff and Federico Faggin
  - *"for the conception, design, development, and application of the first microcomputer, a universal building block that enabled a multitude of novel digital electronic systems"*