NAND Flash and New Applications

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“She Invent” Program In WDC
An introduction

Problem
--21% of our worldwide technical staff is female
--Only 11% of our inventor participation is female

Root Cause
--Information gap
--Confidence gap
--Social norms
--Perfectionism
--Imposter syndrome

Actions
- Increased Invention Review Boards
- Established mentoring programs
- Created training video
- Celebrating female inventors

--Female participation in the patent program increased 27% from FY20 to FY21
--Number of WDC women who submitted inventions increased 29% from FY21 to FY22
Talk Outline

1. Introduction
2. 3D NAND Flash Scaling
3. The Flash Management
4. The Flash Applications
5. Takeaway
Talk Outline

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Worldwide Data Creation

Data Created

ZB

2023 Data Created & Stored

ZB

SOURCE: IDC GLOBAL STORAGESPHERE FORECAST, 2022-2026, APRIL 2022, #US49155722
Storage and Memory Hierarchy

HDD is storage foundation
NAND is not replaceable
Leading Portfolio Breadth and Depth
Solutions to capture, preserve, access and transform data
Talk Outline

1. Introduction
2. 3D NAND Flash Scaling
3. The Flash Management
4. The Flash Applications
5. Takeaway
The Last 34 Years Flash Scaling & Continuing

<table>
<thead>
<tr>
<th>Year</th>
<th>Mbit</th>
<th>Um</th>
<th>Production</th>
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<td>1988</td>
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<td>1.0um</td>
<td>production</td>
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<tr>
<td>1992</td>
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<td>~0.7um</td>
<td>experimental</td>
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<tr>
<td>1995</td>
<td>64Mbit</td>
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<td>production</td>
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2D NAND was Litho Driven

- 1991: 2.5 inch 20MB 35KB/sec $50/MB

3D NAND is Etch Driven

- 2019: 20x16x1mm 1TB microSD™ 450MB/sec

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3D NAND Architecture and Cell
Another dimension to scale – not lithography limited

- 5th Generation – 112-128 Layers
- 6th Generation – 160-176 Layers
The Engine of the 3D NAND Revolution: Charge Trap Cell

Program Performance vs. Gen

2D TLC & 3D QLC Performance

Program Perf
PER PLANE

+20% Per Gen

64L 96L 112L

3D QLC Faster Than 2D TLC

2D TLC

2D NAND

3D NAND

SOURCES: WESTERN DIGITAL ESTIMATES
The Four Vectors of 3D NAND Scaling

**Vertical Scaling**
- Multi-Tiered Memory Hole
- Thinner Memory Layers

**Lateral Scaling**
- Memory Hole Density
- Staggering & Overhead Reduction

**Architecture Scaling**
- Thinner Memory Layers

**Logical Scaling**
- SLC → MLC → TLC → QLC → PLC
Increasing NAND Industry Capital Intensity

CapEx Per 1% Bit Growth

CapEx Per Incremental Bit

Technology Must Be Affordable to Customers

Source: Yole NAND Market Monitor Q1'22
Design Innovations – Addressing Latency
Asynchronous Independent Plane Read (aIPR) – ISSCC 2021

Synchronous Read in Timing
- Plane 0: TLC Read
- Plane 1: TLC Read
- Plane 2: TLC Read
- Plane 3: SLC Read

Asynchronous Read in Timing
- Plane 0: TLC Read
- Plane 1: SLC Read
- Plane 2: TLC Read
- Plane 3: SLC Read

Random Read Performance
- 2-Plane IPR: +82%
- 2-Plane aIPR: +48%
- 4-Plane aIPR:

More Freedom and Less Delay
For Customer to Access Their Data

Sources: Western Digital Estimates
Tradeoffs Everywhere

Cell Performance, Cell Reliability, GB-Cost Have Trade-Off Relationships

- Slow Performance ↔ Larger Vt Window ↔ Better Reliability
- Faster Performance ↔ Smaller Vt Window ↔ Worse Reliability

Vt Window

Vt

Er

A B C D E F G

Larger Die

Smaller Die

512Gb

1Tb

Larger Die ↔ Overhead % ↓ ↔ Cost ↓
Smaller Die ↔ RC-Delay ↑ ↔ Perf ↓

Cost/GB

BETTER

Program Performance
BETTER

Cost Degrades At Faster Performance

Smaller Cell ↔ Stack Height ↑ ↔ Cost ↑
Larger Cell ↔ Proximity Effects ↓ ↔ Perf ↓
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Data Reliability – Paper Analogy

Endurance
How many times can I erase the media and rewrite?

Data Retention
How long can I read the media?
Traditional SSD Hardware Architecture

Traditional (majority) SSD function
Pro:
• Take care all flash management
• Transparent for host to migrate between different flash
Con:
• Host cannot control the performance when internal GC ongoing

FMS 20190806_SSDS-102-1_Marks.pdf
Typical SSD Controller Architecture

- **PCIe/SAS/SATA PHY**
  - PCIe
  - SATA
  - SAS
  - NVMe
  - Sata CMD handler
  - SAS CMD handler

- **Host Selector**
  - CMD XLRFR

- **Host Interface**

- **Processor Sub-System**
  - Processor Core
  - Interconnect Bus
  - Interconnect Data BUS

- **Flash Interface**
  - DRAM
  - ROM
  - UART
  - GPIO
  - Multi-port Arbitor + SRAM controller
  - SRAM
  - LDPC Engines
  - NAND Flash CTRL 01
  - NAND Flash CTRL 02
  - NAND Flash CTRL 03
  - NAND Flash CTRL 04
  - Flash PHY
  - Flash

FMS 20190806_CTRL-102A-1_McIntyre.pdf
Various SSD Control Type

Host System
- Solid State Drive
- Block Meta Data
- Data Buffering
- Wear Leveling
- Error Handling
- Flash Interface
- NAND Media

Host (ZNS)
- Physical Addressing R/P/E
- Solid State Drive
- Block Meta Data
- Data Buffering
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Zone Namespace (ZNS)
- Flash Interface
- NAND Media
Zone Names Space

- The storage device logical block addresses are divided into ranges of zones.
- Writes within a zone must be sequential.
- Different Application will write to different zones.

Device LBA range divided in zones

Zone 0 | Zone 1 | Zone 2 | Zone 3 | ..... | Zone X

Application 1 | Application 2 | Application 3

Conventional SSD Controller
LBA Space

Application 1 | Application 2 | Application 3

ZNS SSD Controller
Zoned LBA Space

Write commands advance the write pointer
Reset write pointer commands rewind the write pointer

Write pointer position

IEDM 2019 Tutorial (Western Digital)—Jian Chen
Error Detection and Correction

BCH → LDPC
## Data Protection—RAID Scheme

### 8 Dies

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Defect rate for 8 die strip</th>
<th>Defect rate for 128 die stripe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Failure rate w/o RAID</td>
<td>1-(1-50ppm)^8 = 400ppm</td>
<td>1-(1-50ppm)^128 = 6400ppm</td>
</tr>
<tr>
<td>Failure rate w RAID</td>
<td>1-(1-50ppm)^8-[1-(1-50ppm)^7]x50ppm = 0.07ppm</td>
<td>1-(1-50ppm)^128-[1-(1-50ppm)^127]x50ppm = 20ppm</td>
</tr>
<tr>
<td>RAID Capacity Overhead</td>
<td>12.5%</td>
<td>0.8%</td>
</tr>
<tr>
<td>Raid overhead</td>
<td>8/7=1.14</td>
<td>128/127=1.007</td>
</tr>
</tbody>
</table>

### 128 Dies

|$FMS\ 20190806\_ARCH-101-1\_Yang.pdf$
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**Compute-Centric Architecture**

**Architecture Bottlenecks**

- Software cannot keep up with IO
- IO interferes with Applications
- Local resources are stranded
- AI/ML/Analytics need to access larger datasets
Evolution of Data Centers
Data-Centricity Will Drive the Architecture

EARLY TO MID COMPUTE-CENTRIC ERA

HYPERCONVERGED INFRASTRUCTURE

DISAGGREGATED INFRASTRUCTURE

POWERED BY THE FUNGIBLE DPU

LATE COMPUTE-CENTRIC ERA

DATA-CENTRIC ERA

FMS 2020 Fungible Keynote

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Need to Get the Bits Out!

- **1GB/s PCIe® 3.0**: 2010
- **2GB/s PCIe 4.0**: 2017
- **4GB/s PCIe 5.0**: 2019
- **8GB/s PCIe 6.0**: 2021

**Host I/F**

- **7 Years**
- **2 Years**

**Node-Over-Node**

- **NAND I/F**
- **>30%**

**Sources:** Western Digital Estimates
4 Main trends in Storage for AI

FMS 2020-Dave Eggleston-Intuitive Cognition Consulting

- **Software**
  - Nvidia GPU direct Storage
  - Weka IO file system

- **Computational Storage**
  - NGD ASIC based SSD
  - ScaleFlux FPGA based SSD
  - Samsung FPGA and ASIC based SSD

- **DPU**
  - Nvidia Bluefield DPU + onboard GPU
  - Fungible DPU

- **Memory Tiering**
  - Huge SRAM –Groq TSP
  - Memory network –IBM Power 10
  - PMEM on DDR channel –Intel + Penguin
CXL Interface

New Applications for AI/ML

- Large Data Space by NAND Flash
- Lower Latency by internal DRAM Cache
- Min. 64 bytes data transfer speed
- AI/ML Application optimized solution

Flash Memory Summit 2022 Samsung Keynote
Computational Storage

• Data is
  – Big
  – Growing
  – Valuable

• Moving data to compute is
  – Expensive
  – Power Hungry
  – Best Minimized

• Move compute to storage
  – Bulk of data crunching in storage
  – Results pass back to CPU

FMS 20190808_COMP-302B-1_Bowen.pdf  Xilinx
ML Accelerator – Compute in Memory (CIM)

- Memory as Multiplication Engine

**Weighted Sums**

\[ Y_j = \text{Nonlinear Activation Function} \left( \sum_{i=1}^{3} W_{ij} \times X_i \right) \]

- Compute in memory as a Matrix Multiplication Units – can be integrated with Digital processors

[CIMU](#)

Programmable SIMD

Compute and Data flow buffers

Input activations

Storage Element

DAC

Analog logic (mul/add/shift)

ADC

psim/ output activations

CPU (Applications)

On-Chip Network

DRAM

CIMU

CIMU

CIMU

CIMU

CIMU

[IEDM2019]
Opti NAND – HDD Product with Flash Inside

Win FMS 2022 Product Award

• Western Digital has reimagined HDDs with OptiNAND technology, which integrates an iNAND EFD with traditional spinning disk drives and incorporates innovative changes to the firmware algorithm and SoC.

• OptiNAND has broken through the conventional boundaries of storage, adding to Western Digital's legacy of industry-first technologies, enabling customers to navigate the phenomenal worldwide growth in data.
Takeaway
Many Innovations in Data Storage

• NAND continue to scale to meet big data demands
  – Technology is viable
  – Need a lot of investment to continue the scaling

• Big Data era need a new architecture to solve the big data problem
  – Data Centric architecture is evolving rapidly

• Computation will move close to data for energy saving
  – A lot new protocols and new architectures are emerging

• More storage and memory are needed in the AI/ML era
References

• IEDM 2019 Tutorial – Jian Chen
• FMS 2019 Programs
• VLSI-DAT Taiwan April 2019 Yan Li
• Tien-Ju Yang and Vivienne Sze “Design Considerations for Efficient Deep Neural Networks on Processing-in-Memory Accelerators”
  • YMTC web site http://www.ymtc.com

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