High-Level Synthesis to Design in the New Millenium

Lauro Rizzatti

Marketing Vice President
Emulation & Verification Engineering (EVE)
lauro@eve-usa.com

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Outline

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- Brief History of EDA
  - Three design paradigm shifts in 40 years
- The SoC Revolution
  - Issues, Trends, Challenges
- High-Level Synthesis
  - What it is
  - Why it is better
- Conclusion

From CAD to EDA

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- **EDA is the crucial technology that enabled and propelled the dramatic growth of today's $1.5 trillion electronics industry**

	70's		80's		90's		00's	
Design Complexity [gates]	5	50	500	5K	50K	500K	5M	50M
Design Abstraction	Discrete		Gates		RTL		Behavioral	
IC Technology	SSI/MSI		LSI/VLSI		ASIC		SoC	
ManufactProcess [um]			3.0	1.0	0.5	0.25	0.10	0.05
Front-End Implementation	Paper & Pencil		Schematic Capture		Logic Synthesis		High-Level Synthesis	
Verification	Paper & Pencil		S/W Simulator		S/W Simulator		S/W Simulator	
Verification					+ Formal Analysis		+ Formal Analysis	
Verification							+ H/W-based Verification	
Back-End Implementation	IC Digitizing		P&R		P&R		P&R	
Output	GDS1		GDS2		GDS2		GDS2	

- **10x Complexity Increase Every 5 Years**
- **3 Design Paradigm Shifts in 40 Years**

Complexity Grows Faster and Faster

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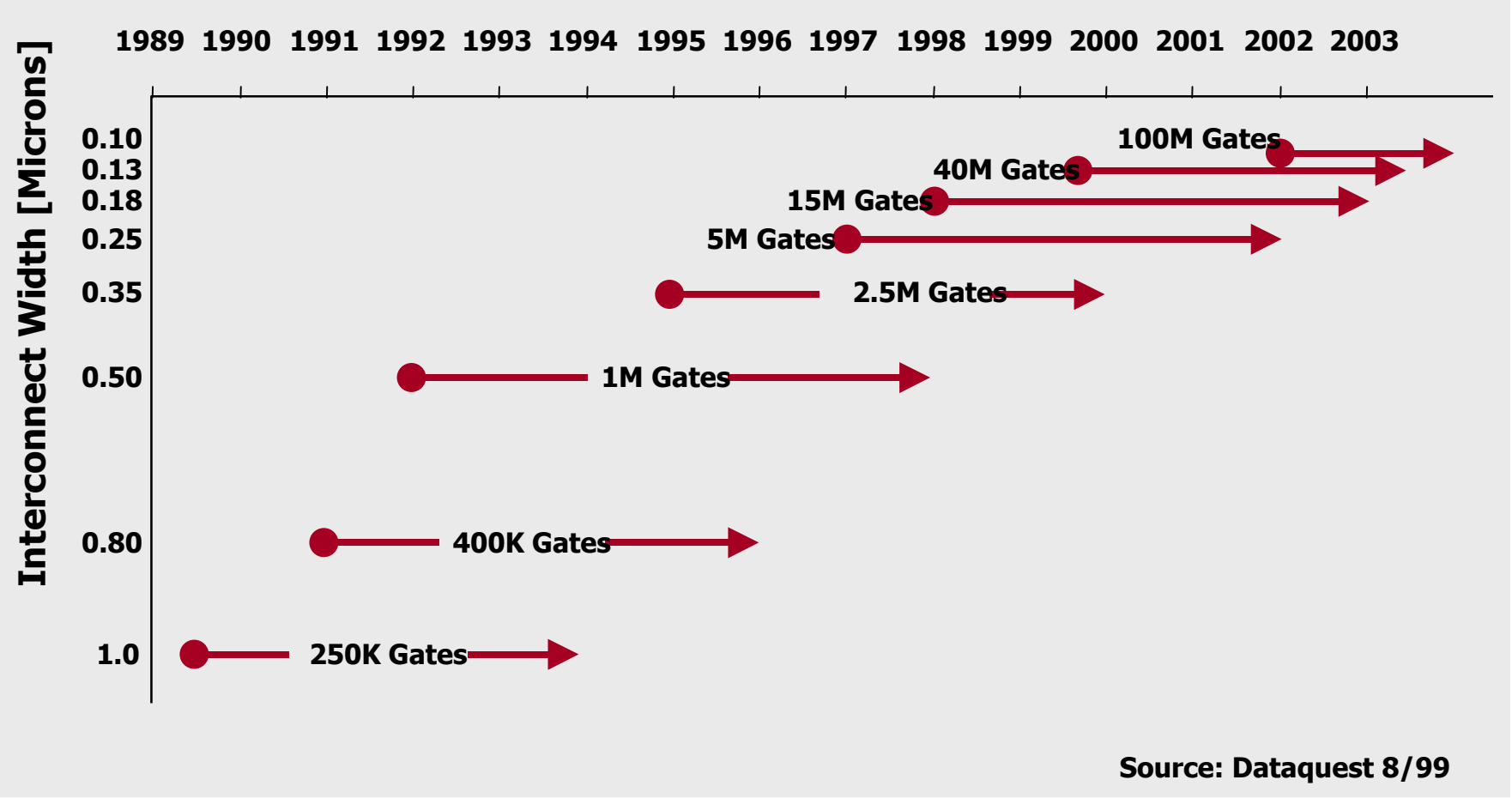

The Productivity Gap is Becoming a Canyon

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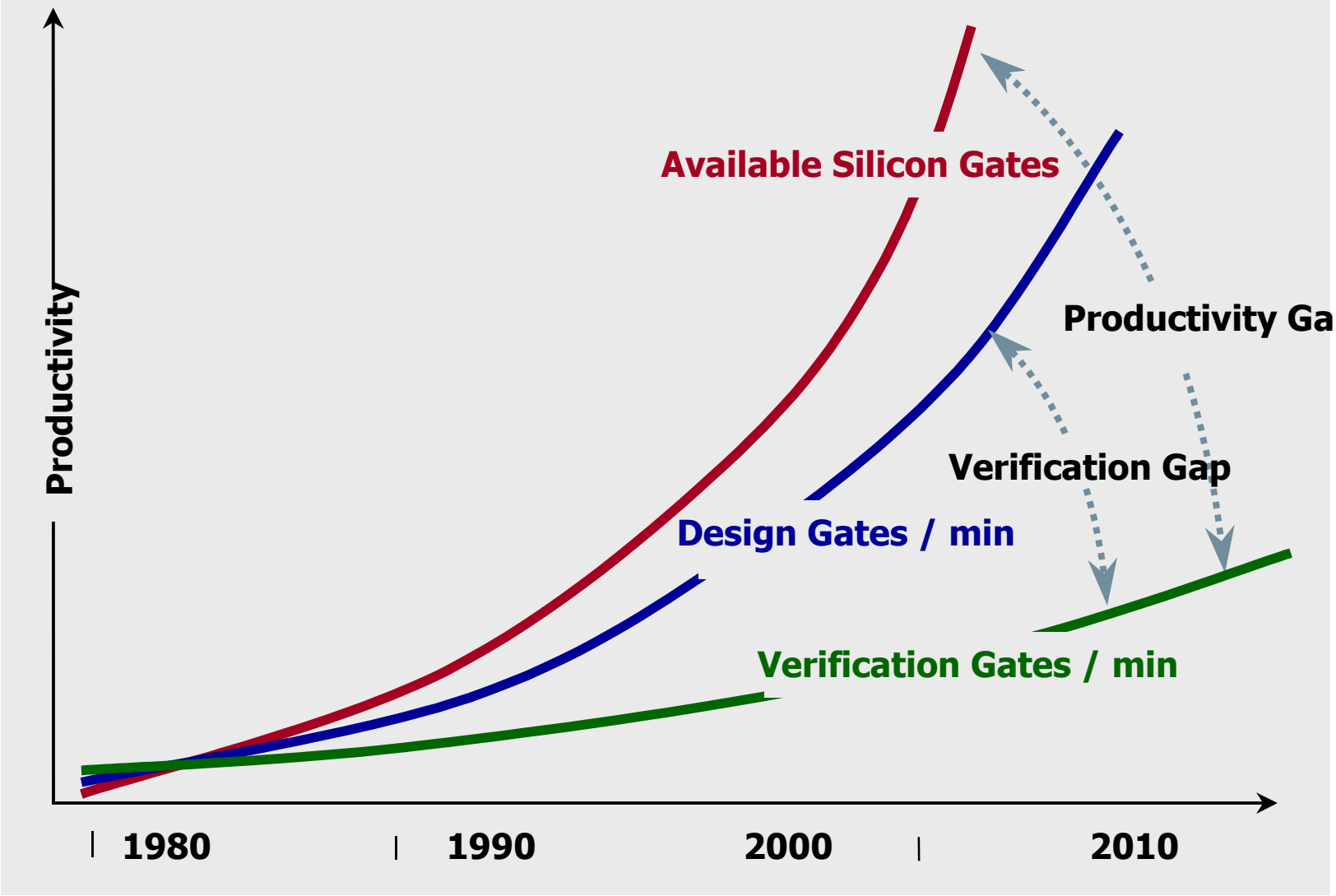
- **Silicon technology is outstripping design capability**



Revenue Loss Because Late to Market

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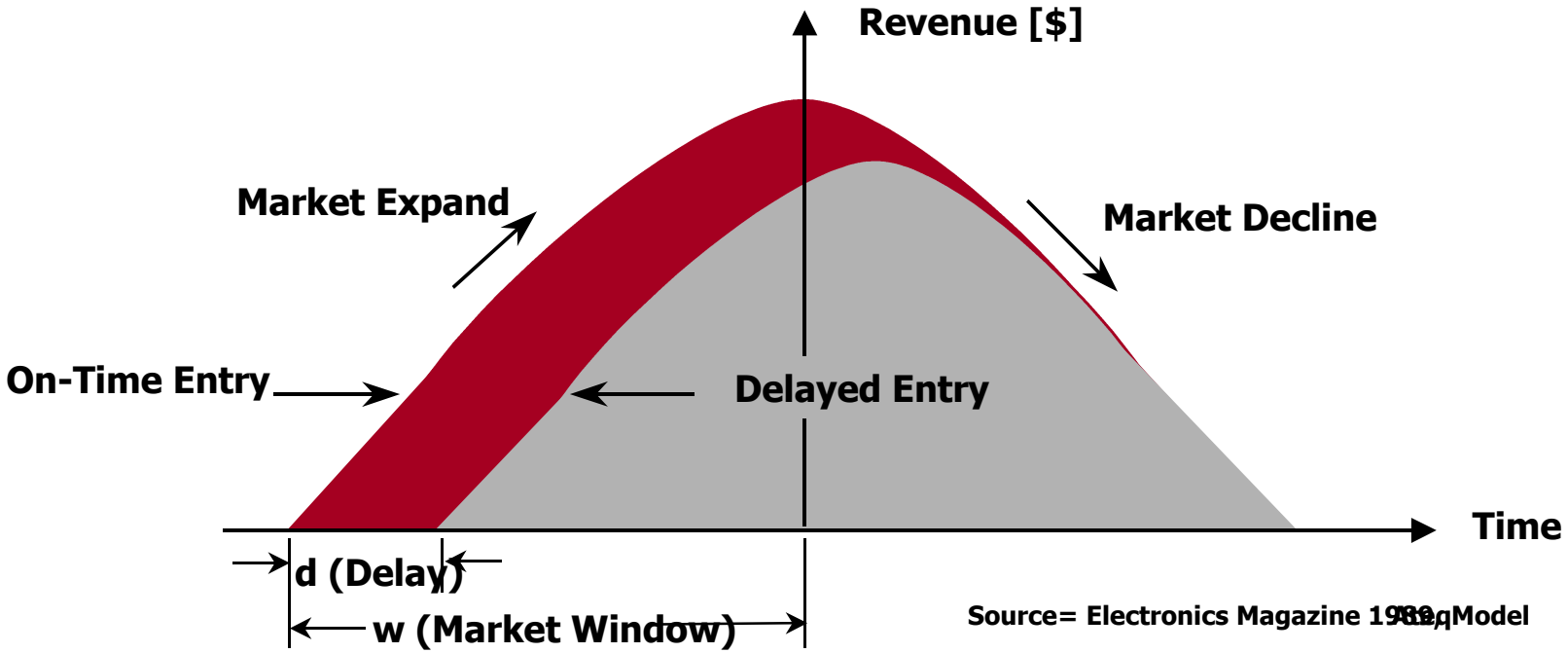

Lost Revenue=Total Expected Revenue $\times \frac{d(3w-d)}{2w^2}$

- **Example**
  - Total Revenue = $200 Million
  - Product Life = 18 Months
  - Revenue Lost = $1 Million/Day

The SoC Revolution

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- **Productivity Issues in SoC Design**
  - **System-level design is very cumbersome**
  - **Exploring alternative architectures**
  - **Addressing performance requirements (timing, area and power) earlier in the design flow**
  - **Capability to design/describe complex blocks**
  - **Transparent memory interfacing**
  - **Tool capacity and synthesis throughput**
  - **Effective design reuse**
  - **Design turnaround-time**

SoCDesign Challenges

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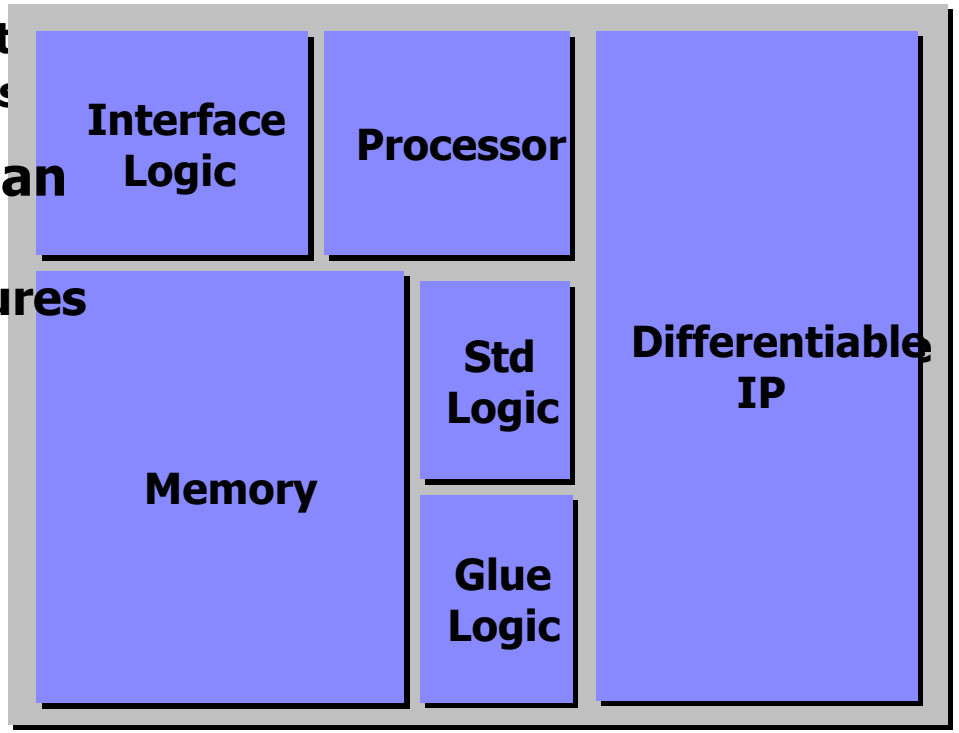
- SoCdesign model is very similar to a PC-board design model
  - Processor is proprietary
  - Memory is a commodity
  - Standard/interface logic is interchangeable and price sensitive
  - IP Blocks are Key Differentiators in SoC
    - High throughput
    - Complex, Algorithmic functionality
    - Contains arithmetic computations
- Chip complexity 100x larger than in 1990
  - Front-end design tool architectures of the 90's are breaking
  - Methodology level too low for complex chip designs
  - Very hard to converge to meet timing goals
  - System-level designers too far away from ASIC design process



Electronic Design Automation Flow

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System Design

Register-Transfer-Level [RTL]

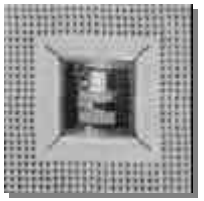
Logic Design

Gate-Level Netlist

Physical Design

GDS-II

Process Technology



Current Design Methodology Flow

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Specification/Functional Modeling

Micro-Architecture

System Design

RTL Coding

Time Budgeting/Synthesis Scripting

Logic Design

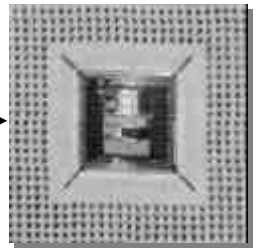
RTL Synthesis

Datapath Synthesis

Logic Synthesis

Floor-Planning

Place and Route



Design Methodology Flow based on HLS

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Specification/Functional Modeling

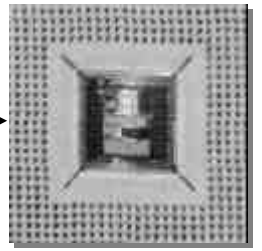
System Design

HL Synthesis

Logic Design

Floor-Planning

Place and Route



High-Level Synthesis vs RTL Synthesis

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Design Step	High-Level Synthesis	RTL Synthesis
• Design Functionality	• Manual by Designer	• Manual by Designer
• I/O Behavior	• Manual by Designer	• Manual by Designer
• Register Insertion	• Automatic, timing-driven	• Manual, "logical" locations
• Micro-Architecture Creation (throughput, latency, RAM interface, serial or parallel architecture , etc.)	• Automatic, designer guided	• Manual by Designer
• Performance Estimation	• Automatic, technology specific	• 'Guesstimation'
• FSM Generation	• Automatically implemented	• Manual by Designer
• Resource (adders, memory ports, etc.) Selection	• Automatic	• Manual by Designer

High-Level Synthesis Benefits

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- **Intuitive Coding**
  - **Up to 10X fewer lines of code**
- **Architectural Exploration**
  - **Fully automatically**
- **Predictable Timing - Area - Power**
  - **Achieve better quality of results**
- **Easy to Analyze and Control**
  - **Designer still in control**

The Right Technology to Enable System Level Design

Conclusion

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- HLS to keep up with Moore's Law
- HLS to enable higher level of abstraction for system-level design
- HLS to implement better designs, in shorter time